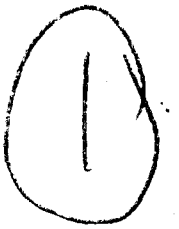

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

THEORY AND IMPLEMENTATION OF A VLSI STRAY INSENSITIVE SWITCHED CAPACITOR COMPOSITE OPERATIONAL AMPLIFIER

by

Raphael Anestis

June 1994

Thesis Advisor: Sherif Michael

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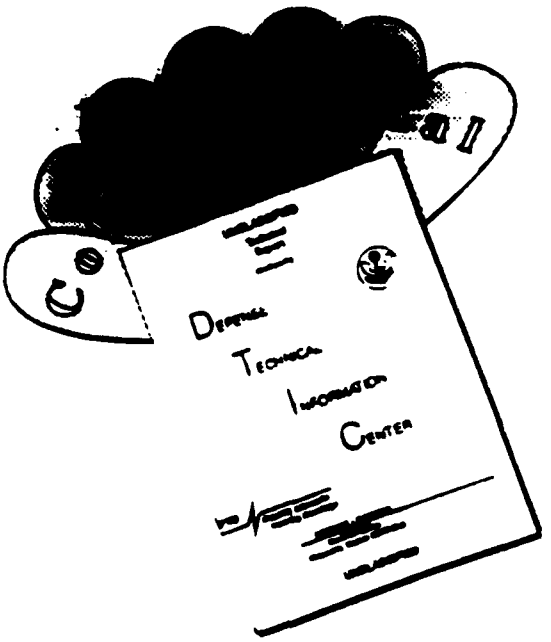

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In this research, analog active circuits are implemented in VLSI technology by combining the properties of switched capacitors and composite amplifiers. This combined design solves the problems of the single operational amplifier (OA) such as finite dc gain, limited bandwidth and lower slew rate, as well as enhancing the overall network passive and active sensitivities. For the first time, a theoretical analysis was conducted in a newly-defined discrete transform domain. The analysis was used to justify the circuits that were first designed in the resistor domain and also debug the initial attempts that were made to build an analog chip. The switched capacitor design is implemented using both the toggle switched inverter and the modified open floating resistor techniques. The composite OA is implemented using the C-2OA-1 design out of all the CNOA-i possibilities. The two alternatives, together with two single CMOS OAs that were added for comparison reasons, are produced on a single analog/digital microchip. The digital part includes the two phase non-overlapping clock and programmable switches. It is isolated from the analog part using a low-noise design technique. Sufficient simulations were made to anticipate results in positive and negative finite gain configurations, and also to evaluate the two different techniques. Finally, neural networks applications of the chip are suggested evoking thoughts for the advantages of this promising domain.

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Theory And Implementation Of A VLSI Stray Insensitive Switched Capacitor Composite Operational Amplifier

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Submitted in partial fulfillment
of the requirements for the degrees of

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ABSTRACT

In this research, improved analog circuits are implemented using VLSI technology by combining the properties of switched capacitors and composite amplifiers. This combined design solves some of the problems of the single operational amplifier (OA) such as finite dc gain, limited bandwidth and lower slew rate, as well as enhancing the overall network passive and active sensitivities. For the first time, a theoretical analysis was conducted in a newly-defined discrete transform domain. The analysis was used to justify the circuits that were first designed in the continuous domain and also debug the initial attempts that were made to build an analog chip. The switched capacitor design is implemented using both the toggle switched inverter and the modified open floating resistor techniques. The composite OA is implemented using the C2OA-1 design out of all the CNOA-i possibilities. The two alternatives, together with two single CMOS OAs that were added for comparison reasons, are produced on a single analog/digital microchip. The digital part includes the two-phase non-overlapping clock and programmable switches. It is isolated from the analog part using a low-noise design technique. Sufficient simulations were made to anticipate results in positive and negative finite gain configurations, and also to evaluate the two different techniques. Finally, neural networks applications of the chip are suggested evoking thoughts for the advantages of this promising technique.

TABLE OF CONTENTS

I. INTRODUCTION

A. OVERVIEW

The operational amplifier (OA) is one of the most important analog integrated circuits since it has widespread use throughout most applications. Its popularity explains the literally hundreds of OAs available, offering various performance trade-offs. Speed, accuracy, gain and bandwidth are some of the trade-offs, and their investigation challenges the technology progress. Furthermore, the possibility of its implementation using a Very large Scale Integrated (VLSI) process, with feature sizes in the vicinity of 1 μm, increases the packing density, with subsequent decreases in the cost of complex integrated circuits.

The Composite Operational Amplifier (CNOA-i), where N is the number of OAs in the design, is a compact design circuit that considerably improves most limiting factors in the non-ideal performance of the OA. Combining the CNOAs in a parasitic-free switched-capacitor network allows for circuit implementation on a single VLSI chip, as well as providing considerable performance improvement and bandwidth extension over the single OA. This combination has direct applications in A/D and D/A conversion, digital communications, filtering, signal processing, speech processing, modulator-demodulator circuitry, HDTV, and neural network implementation, to name a few.

This thesis proposes to conduct for the first time a theoretical analysis using a newly defined discrete transformation. The purpose is to mathematically justify the advantages of the initial analog circuit when combined with switched capacitors into a single stray insensitive design, and also to debug the first attempts that were made to build an analog chip. The microchip implementation will be realized using a low-noise VLSI full-custom process. Thus, this thesis intends to offer a complete methodology about designing switched capacitor analog/digital microchips, and then reveal their advantageous use in increased accuracy, small area, neural networks applications.

B. EXISTING PROBLEMS AND SOLUTIONS

For the theoretical foundation of circuits, one stumbles into the derivation of transfer functions that may be very complicated and that can be handled only with an advanced mathematical software package in order to minimize the human error probabilities.

For the VLSI implementation, the amount of noise injected from the digital portion of the circuit must be isolated from the analog part. This leads to the application of special design techniques, layout topologies, and the use of a fabrication process optimized for analog/digital microchips. Latchup is another problem one, which is prevented by use of substrate contacts of the appropriate type in every well and some other relatively simple design considerations.

Finally, maximum information will be extracted, using the available simulation tools, such as *SPICE*.

C. THESIS ORGANIZATION

The goal of this thesis was to standardize the steps that lead from the design and mathematical evaluation to the fabrication of a stray insensitive switched capacitor composite operational amplifier on a single CMOS microchip. The use and limitations of all operational amplifiers will be discussed in the second chapter. The CMOS operational amplifier is going to be briefly introduced in the third chapter and compared to the bipolar amplifier. The generation of composite operational amplifiers will be explained in the fourth chapter. Switched capacitor networks will be presented in the fifth chapter. The sixth chapter will analyze in detail all the theory behind the switched capacitor composite amplifier C2OA-1, and will derive the different configuration transfer functions. The difficulties faced, the given solutions, and the complete implementation of the microchip are discussed in the seventh chapter. The applications of the switched capacitor and analog VLSI philosophy into the promising domain of neural networks are listed in the eighth chapter. Finally, conclusions developed from this thesis are presented in the ninth chapter along with recommendations for future research.

II. OPERATIONAL AMPLIFIERS

A. WHAT IS AN OP AMP, WHERE AND WHY IT IS USED?

Although the variety of standard and special-purpose custom integrated circuits that fall into the analog category is almost limitless, a few standard circuits stand out as perhaps having the widest application in systems of various kinds. These include operational amplifiers (OAs), voltage regulators, phase-locked loops, and A/D and D/A converters. In this chapter, the importance of the operational amplifier will be underlined. Most analog integrated circuits consist primarily of OAs connected in such a way as to perform the desired function.

An ideal operational amplifier is a differential input, single-ended output amplifier with infinite gain, infinite input resistance, zero input reactavce, and zero output impedance. The general-purpose bipolar monolithic operational amplifier type 741, which is shown in Figure 2.1, has been used in various different configurations or setups. In Figures 2.2, 2.3, 2.4, 2.5, 2.6, 2.7, and 2.8 respectively, we see the inverting, non-inverting, voltage-follower (or buffer), differential, logarithmic, integrator and differentiator configurations, which are some of the most important in building analog blocks. The widespread use of the OA can be traced to the ease of understanding its parts. It behaves much like the ideal characteristics, a fact that makes it easy to implement a given design.

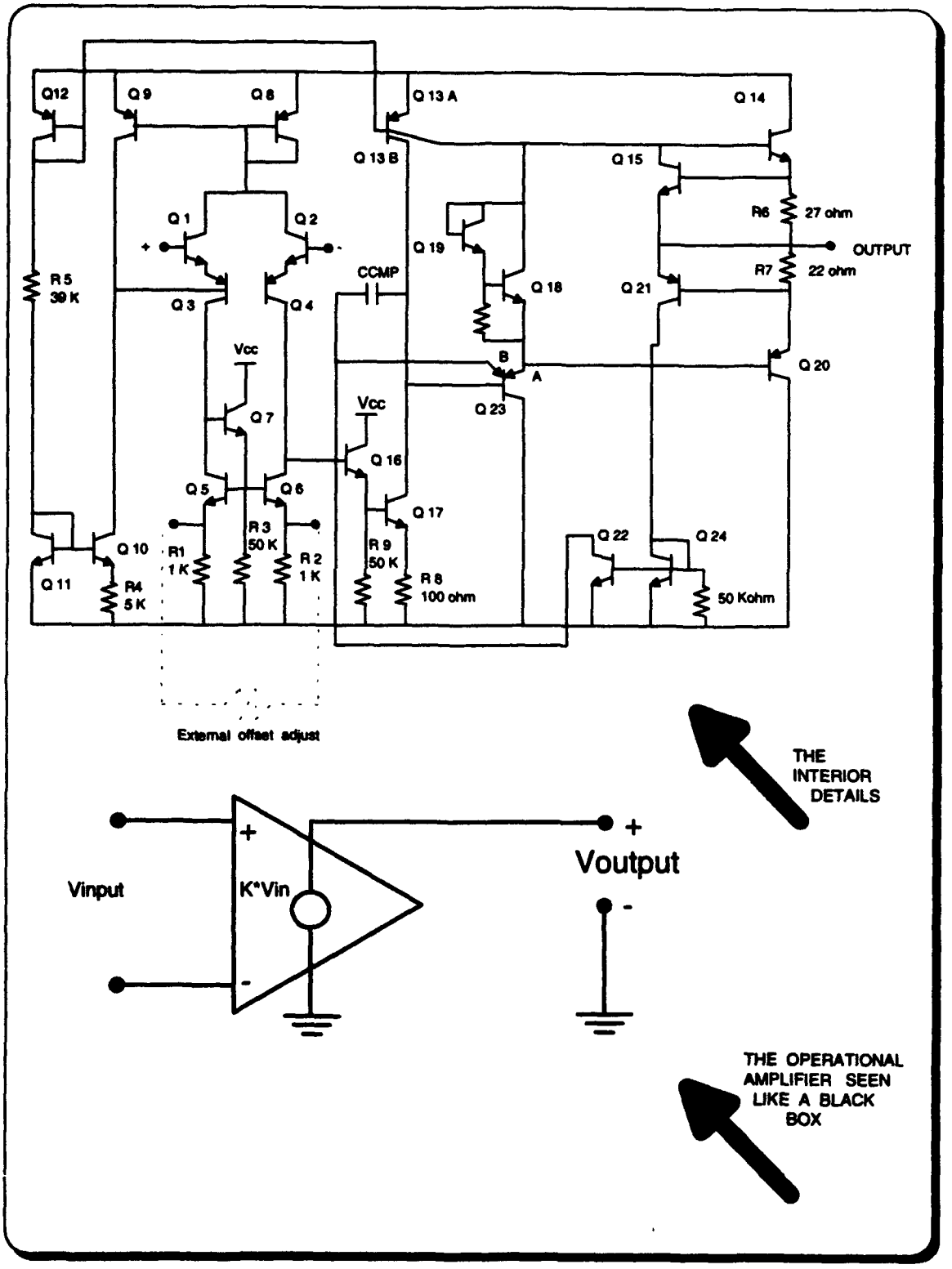


Figure 2.1 741 Operational Amplifier Circuit

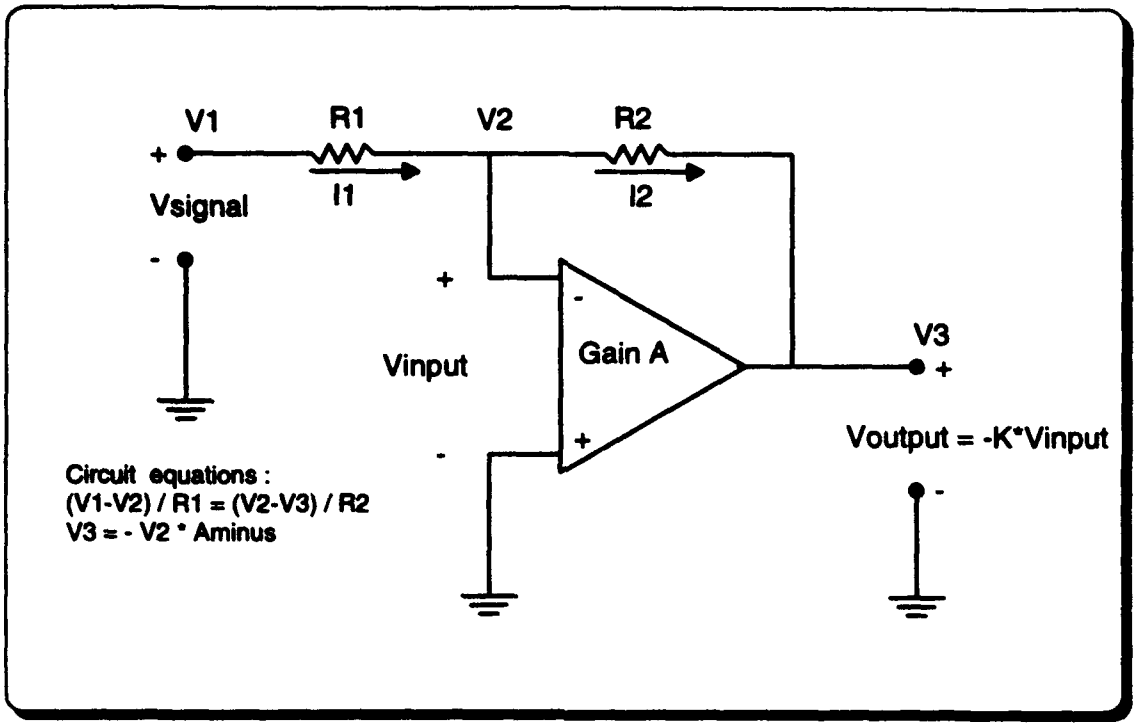


Figure 2.2 Inverting Amplifier Configuration

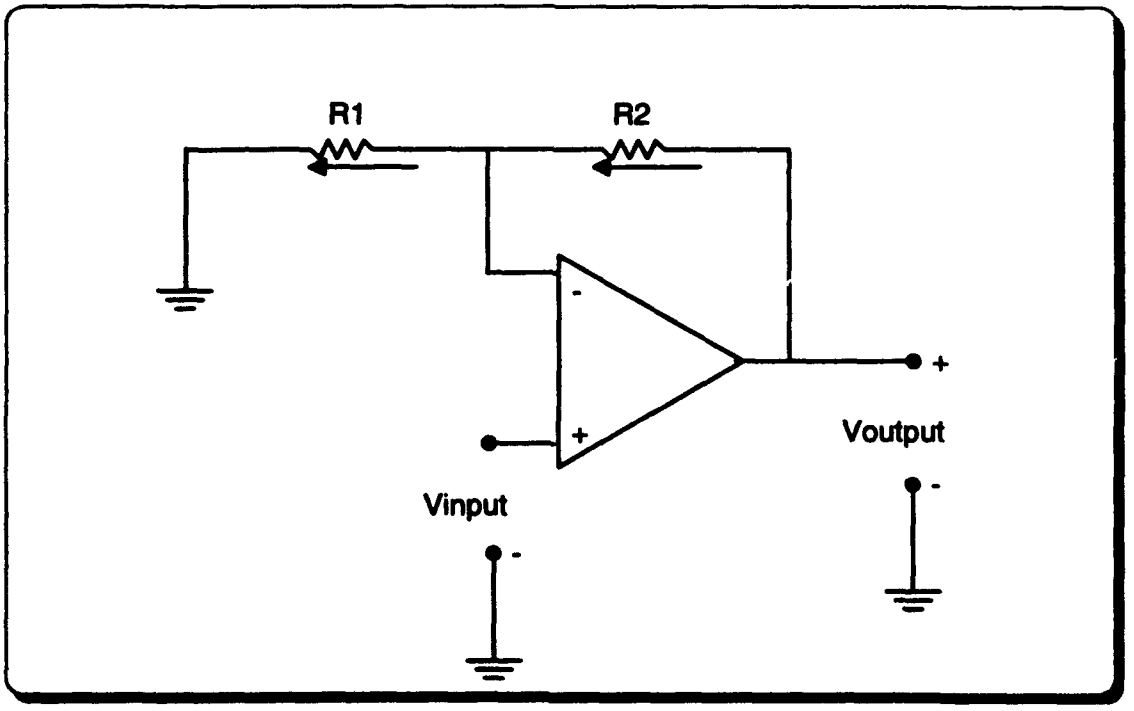


Figure 2.3 Non-inverting Amplifier Configuration

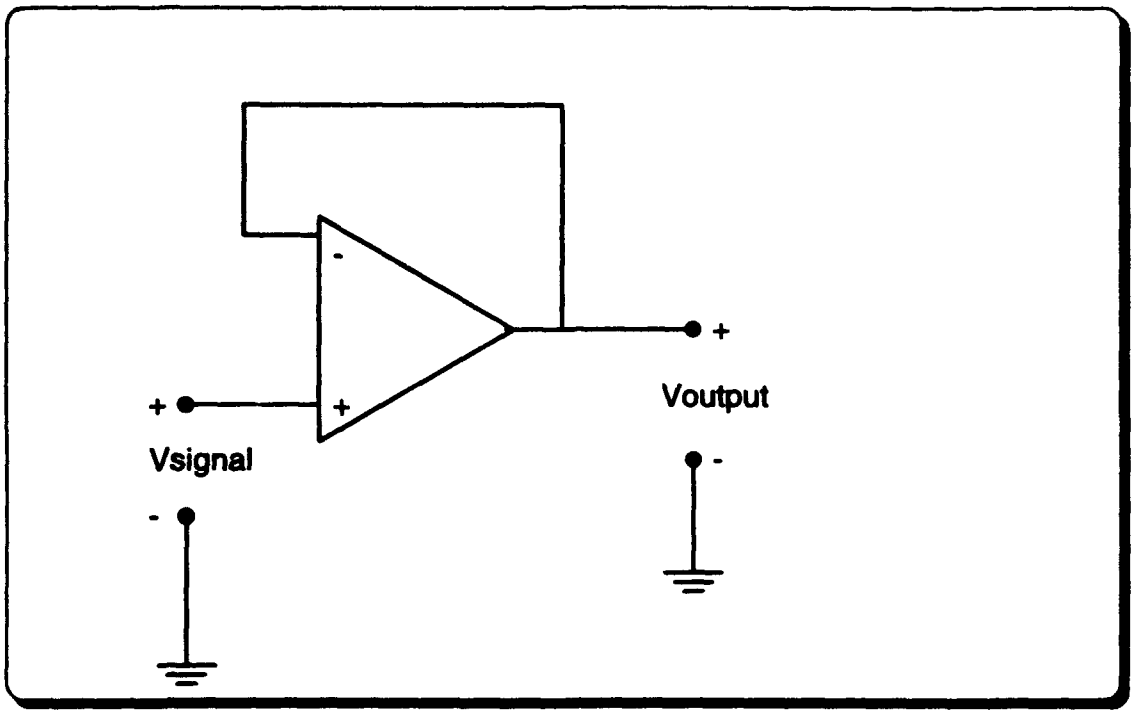


Figure 2.4 Voltage Follower Configuration

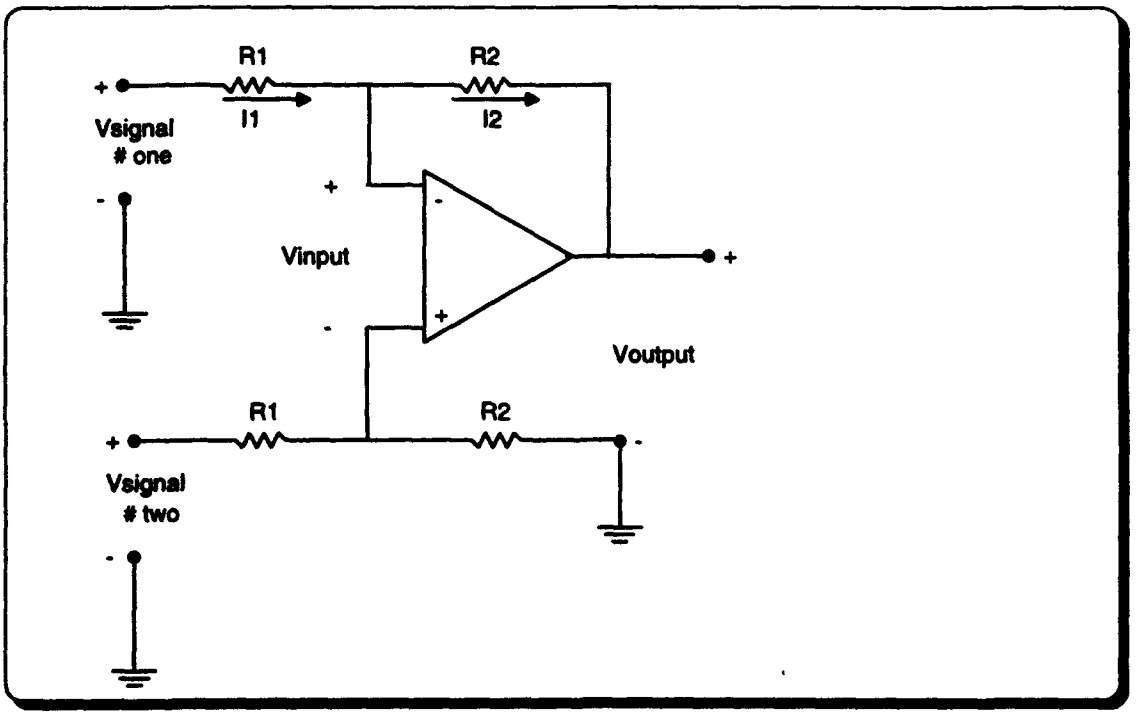


Figure 2.5 Differential Amplifier Configuration

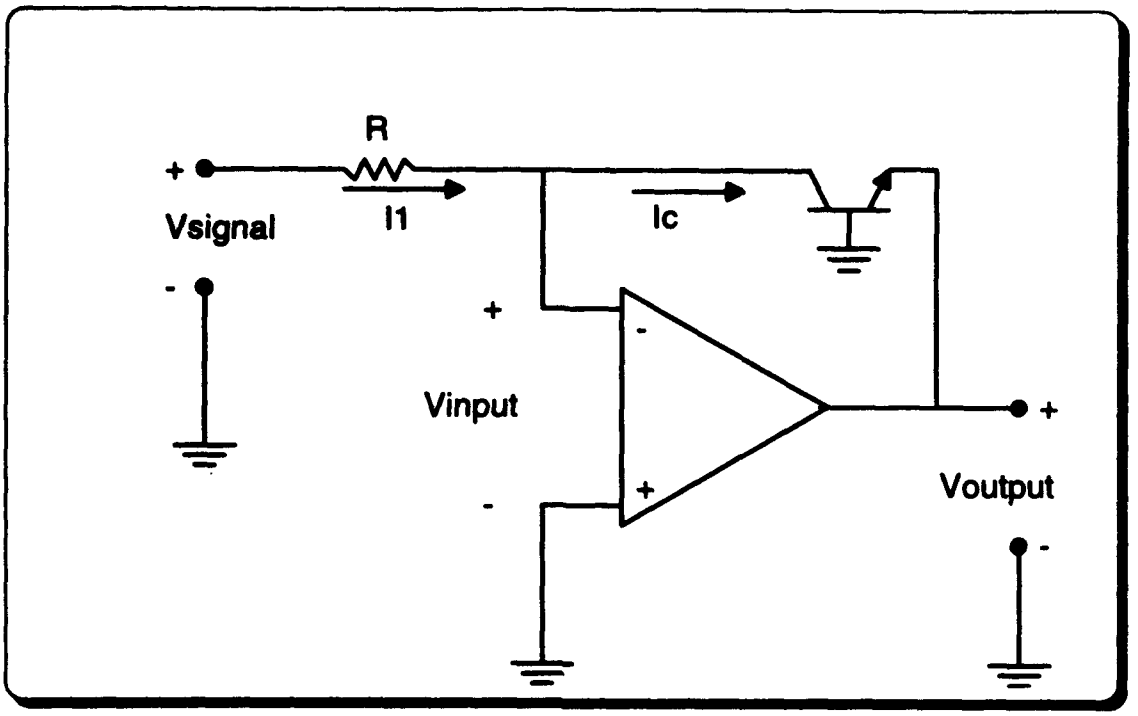


Figure 2.6 Logarithmic Amplifier Configuration

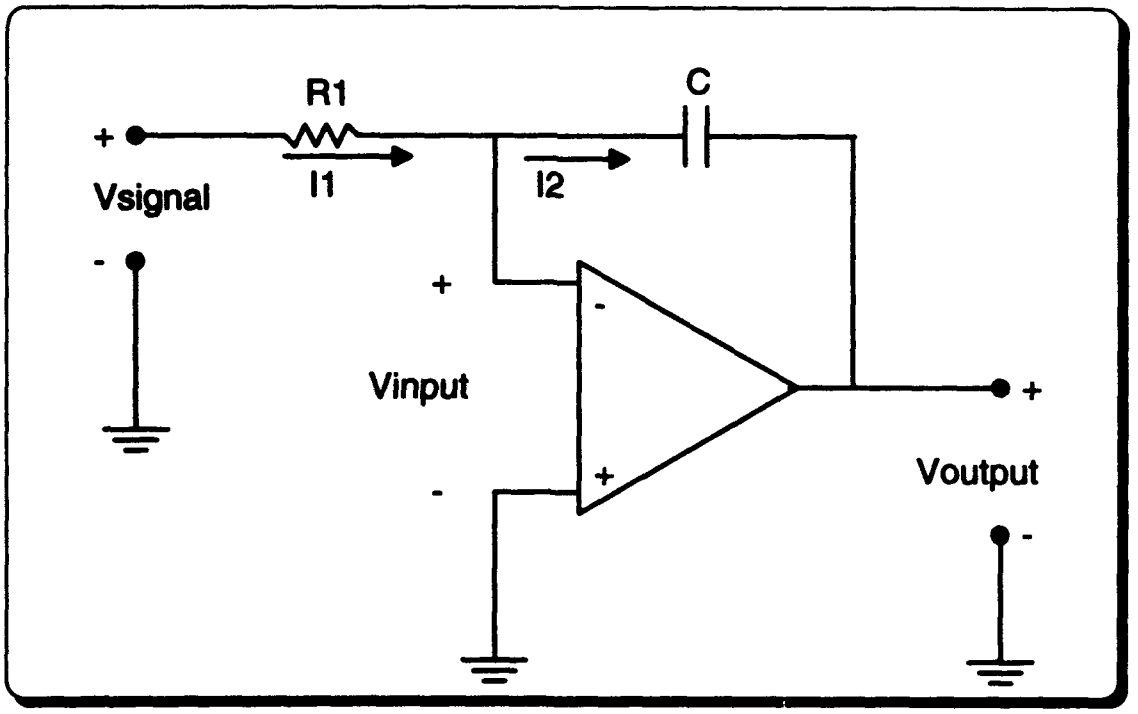


Figure 2.7 Integrator Configuration

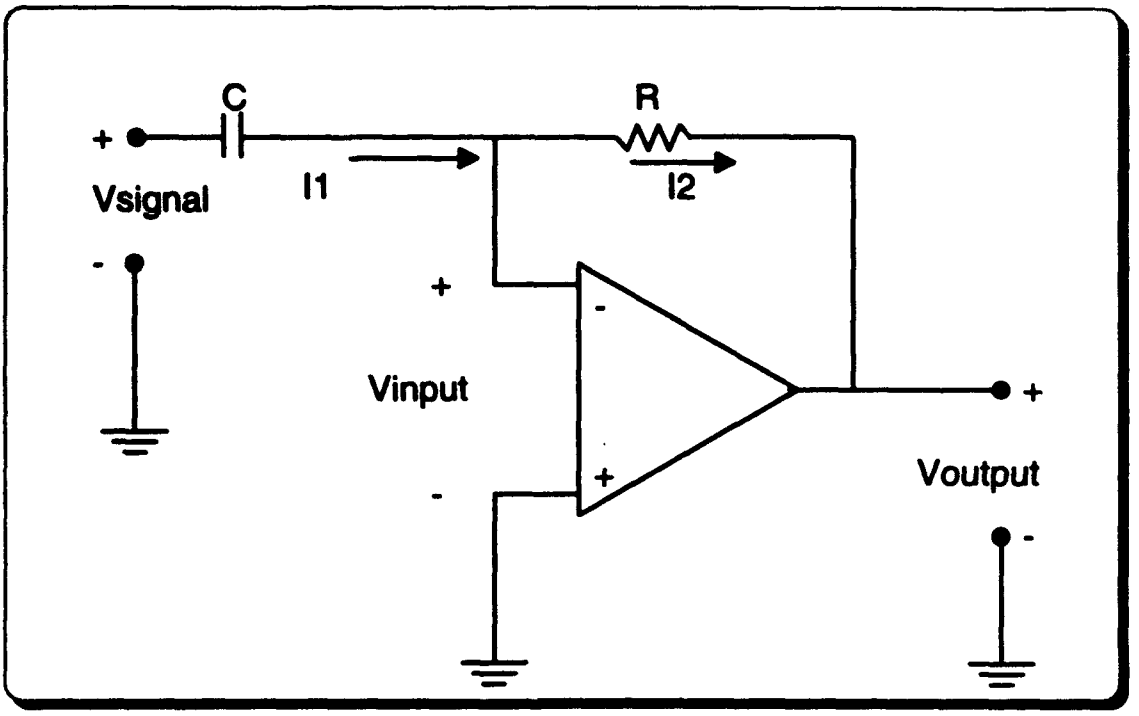


Figure 2.8 Differentiator Configuration

B. INTRODUCTION TO FEEDBACK CONCEPTS

Virtually all operational amplifier applications rely on the principles of feedback. The generalized feedback amplifier is shown in Figure 2.9. The block labeled K is called the forward or basic amplifier, and the block labeled F is called the feedback network. The gain of the amplifier, when the feedback network is not present, is called the *open-loop gain (K)* of the amplifier. The function of the feedback network is to sense the output signal (Sout) and develop a feedback signal (Sfb), which is equal to F*Sout, where F is usually less than unity. This feedback signal is subtracted from the input signal Sinp, and the difference Serr is applied to the basic amplifier.

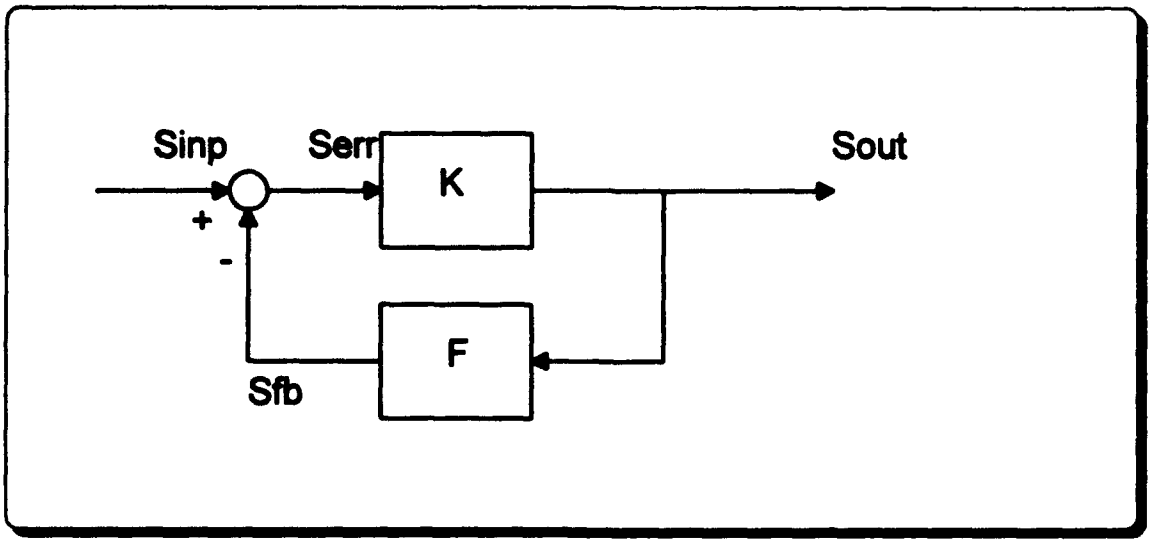


Figure 2.9 A Conceptual Feedback Amplifier

The gain of the system when the feedback network is present is called the closed-loop gain. The transfer function is

$$\frac{S_{out}}{S_{inp}} = \frac{K}{1+K*F} \tag{2.1}$$

where as the product of K*F, which is called the *loop gain T,* becomes very large then

$$\lim_{K*F\to\infty} \frac{K}{1+K*F} = \frac{1}{F} \tag{2.2}$$

Since the feedback network is composed of passive components, the value of F can be set to an arbitrary degree of accuracy and will establish the gain at a value of 1/F, independent of any variations in the *open-loop gain (K)* (This is the ideal case, in reality we need to internally compensate in order to maintain the desired stability). This independence of the closed-loop performance, from the parameters of the active amplifier, is the primary motivating factor in the wide use of operational amplifiers as active elements in analog circuits.

C. DEVIATIONS FROM IDEALITY IN REAL OPERATIONAL AMPLIFIERS

Real operational amplifiers deviate from ideal behavior in significant ys. The principal effects of these deviations are the limits in the frequency range of the signals that can be accurately amplified, the placement of a lower limit on the magnitude of a dc signal that can be detected, and of an upper limit on the independence magnitude of the passive elements that can be used in the feedback network with the amplifier. The following list is a summary of the non-ideal characteristics, which are analytically presented in reference 15.

1. Input bias current

Theoretically, input bias current should be zero. Typical values are 10 to 100 nA for bipolar input devices, 1 to 10 pA for JFET input devices and less than 0.001 pA for MOSFET input devices.

2. Input offset current

The current which when applied at the input, provides a zero output current is called input offset current. For the emitter-coupled pair, the two input bias currents will be equal only if the two transistors have the same beta (β) parameters. This aspect of circuit performance is characterized by the input offset current, defined as the difference of the two base currents.

3. Input offset voltage

Input offset voltage is the voltage which when applied to one of the inputs of the OA, produces a zero output voltage. It ranges from 0.1 to 2 mV for bipolar input devices and 1 to 20 mV for FET input devices.

4. Common mode rejection ratio (CMRR)

Theoretically the CMRR should be infinity. For a CMRR of 10^4, or 80 dB, a 10 Volt common-mode signal produces a 1 mVolt change in the input offset voltage, according to the equation

$$CMRR = \frac{differential\ mode\ gain}{common-mode\ gain} \approx \left(\frac{\theta V_{input\ offset}}{\theta V_{common\ mode\ input}} \Big|_{V_o=0}\right)^{-1} \qquad (2.3)$$

The CMRR is usually expressed in dB (multiplied 20 times the logarithm of the ratio), and is a measure of an operational amplifier's ability to reject signals such as noise that is which are simultaneously present at both inputs.

5. Input impedance

Input impedance is the ratio of input voltage to input current. Theoretically, it should be infinity. Typically, it ranges from 100 KΩ to 2 MΩ.

6. Output impedance

Output impedance is the ratio of open-circuit output voltage to short circuit output current. Theoretically, it should be zero. Typically, it ranges from 40 to 100 Ω.

7. Frequency response

The bandwidth of an operational amplifier is the range of frequencies over which the device is able to provide its rated gain. Due to the

existence of parasitic capacitances, the open-loop transfer function of an OA has additional poles which negatively effect the phase margin. The process of modifying the open-loop transfer function A(s) of an OA having three or more poles so that the closed-loop amplifier is stable for any desired value of closed loop gain is called compensation. The simplest and most common method is to reduce the bandwidth of the amplifier (often called narrowbanding). That is, a dominant pole is deliberately introduced into the amplifier to force the phase shift to be less than -180^{0} when the loop gain is unity. This involves a direct sacrifice of the frequency capability of the amplifier, and is realized by adding capacitance, usually between the collectors of the input stage [Ref. 15 : pp 607 - 613].

8. Slew rate

Slew rate is the rate of change of the output voltage with time, in response to a perfect step-function input. Typically, it is on the order of a few volts per micro second.

9. Finite DC gain

Theoretically, finite DC gain should be infinity. Actual values range from 100 to 10^{6}.

10.Finite linear range

Finite linear range is the maximum value for the output voltage without clipping, and is usually limited to a few volts below the dc supply voltage applied.

III. MOS OPERATIONAL AMPLIFIERS

A. MOS INTEGRATED CIRCUITS, ADVANTAGES AND USE

MOS integrated circuits are ICs whose circuitry utilize only MOSFET (metal-oxide-semiconductor field effect transistors) devices with virtually no resistors, diodes, bipolar transistors, or other components. Their popularity is rapidly increasing because MOSFET elements permit greater *complexity* than bipolar elements. This means more *circuitry* and hence more gates and flip flops in the same *area* of a semiconductor chip. This ability to jam more functions into a tiny piece of silicon " real estate ", is the key to more economical integrated circuits. Indeed , this continuing trend toward greater and greater complexity is an important key to progress in electronics. As far as the function of the MOSFET is concerned, one can simply say that it behaves much like a PNP transistor. But, whereas the PNP transistor is turned on by current applied to the control terminal (the base), the MOSFET is turned on by voltage applied to its gate. The name " field effect " applied to this type of transistor refers to the way it is turned on by the effect of the electric field created by the gate voltage [Ref. 28].

The use of MOS transistors as load elements, in place of resistors, and because the MOSFET requires a much smaller silicon area than a BJT, MOS amplifiers can be economically implemented in Very Large Scale Integrated Circuits (VLSI).

B. CLASSIFICATION OF MOS AMPLIFIERS

There are basically two different MOS integrated circuit technologies, NMOS and CMOS. NMOS refers to MOS integrated circuits that are based entirely on *n-channel* MOS transistors. The majority of these transistors are of the enhancement type ; depletion-type transistors are used mostly as load devices. Complimentary MOS (CMOS) technology is based on using both n-channel and p-channel devices, all of which are of the enhancement type. The availability of both device polarities makes it easier to design high-quality circuits in CMOS. In fact, at the present time, CMOS is by far the most popular technology for digital integrated circuits and is rivaling bipolar technology for analog applications. The NMOS technology, though not as convenient for the circuit designer, currently offers the highest possible functional density, a very fast silicon implementation and it requires fewer processing steps than CMOS. Both are used in the design of VLSI circuits. For this research, the use of the CMOS technology has been chosen. As it will be explained later, the purpose of the technology used is to fulfill the needs for an analog sampled data system. The reader may know that the BiCMOS technology is also very attractive because one can get combined advantages , but this is outside the scope of this investigation.

C. DERIVATION OF MOS AMPLIFIERS FROM BIPOLAR.

The basic topology used for most bipolar-transistor OAs is shown in simplified form in Figure 3.1. A differential input stage drives an active load, followed by a second gain stage. An output stage may be added for driving heavy loads off-chip. One must note that in the case of the 741 OA, high performance npn devices are added to improve the performance of the lateral pnp devices in the input stage.

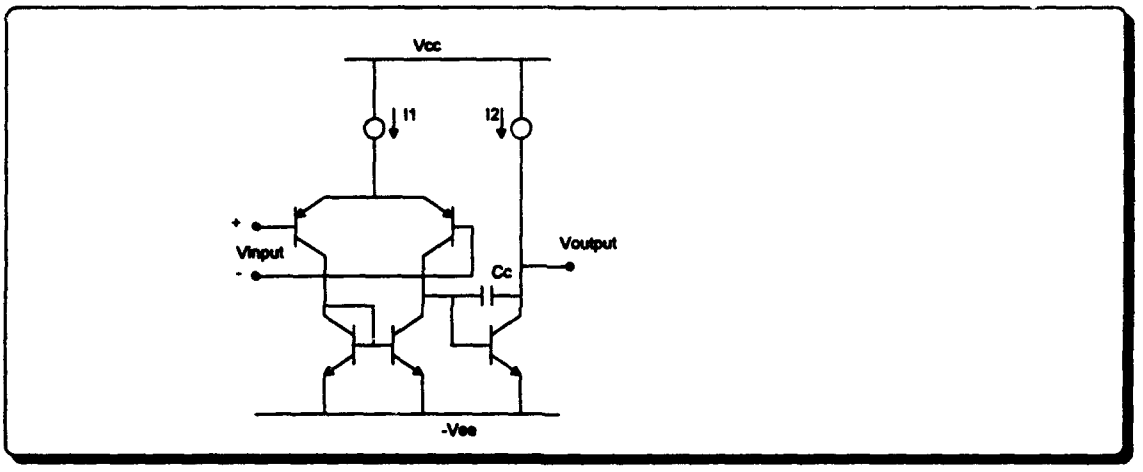


Figure 3.1 Bipolar Implementation of a Two Stage OA

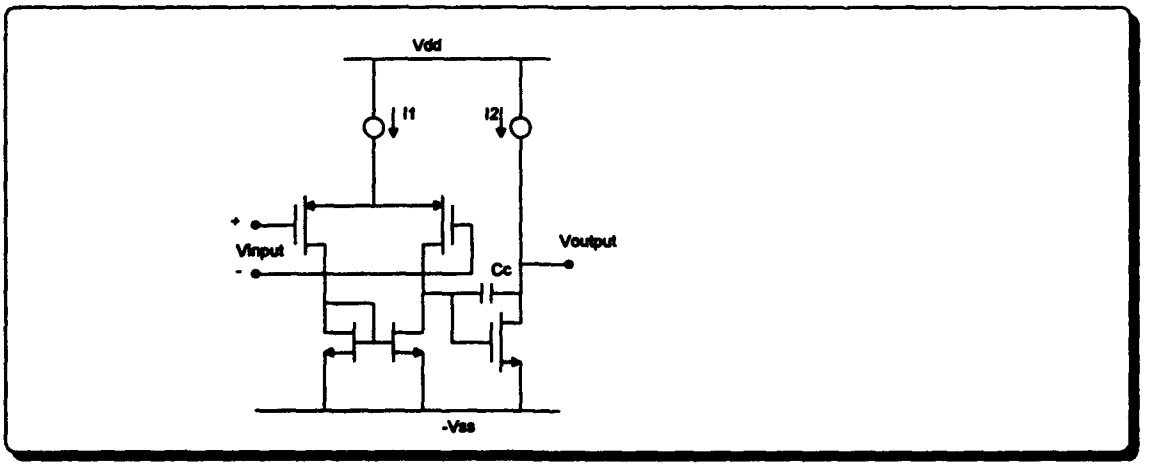


Figure 3.2 CMOS Implementation of a Two Stage OA

The most widely used approach for the implementation of CMOS OAs is derived from Figure 3.1 and is shown in Figure 3.2. This circuit configuration provides good common-mode range, output swing, voltage gain, and CMRR in a simple circuit that can be compensated with a single capacitor.

The voltage gain of the CMOS amplifier can be found by considering the two stages separately, since the second stage is not loading the first stage due to the essentially infinite input impedance of the MOS devices. The overall voltage gain is a strong function of the bias point chosen for the devices and the channel length of the transistors used. This means that we can increase it by either increasing the channel length of the devices used or by reducing the bias current. Both of these changes degrade the frequency response of the amplifier. Thus, fundamental trade-offs occur between frequency response, gain and offset voltage in CMOS OA design.

Several alternative circuit approaches have evolved that optimize certain aspects of the performance of the amplifier. These are :

(1) Improving voltage gain by using cascodes;

(2) Use of common-source-common-gate amplifiers.

D. PERFORMANCE COMPARISONS

As stated before, one of the main reasons that we prefer the CMOS operational amplifiers is the ease they offer in the design of integrated circuits and the reduction in size. But, what about the rest of their non-ideal characteristics compared to bipolar amplifiers ? The available comparison data are listed in Table 3.1.

As one can see from the this Table, bipolar operational amplifiers are better than CMOS in some aspects. This is especially true in gain which is larger, and noise which is ten times lower, than CMOS. They are worse in the input bias current and input impedance. In practice, MOSFET gates, when connected through package pins to the outside world, must be protected against damage by static electricity. This is typically achieved by connecting back-biased clamping diodes from supply and ground to the gate. Thus, the effective input leakage currents are determined by the junction leakage and are of the order of picoamps even for MOSFETs. However, there is no need for protection in the internal design of the chip, and MOSFET amplifiers do realize their inherent ultra-low input-bias currents. As it will be explained in the next chapter, these specific advantages of the CMOS OAs make them an important class of integrated circuits, necessary for use in single-chip switched capacitor filters and other sampled data analog systems.

TABLE 3.1 CMOS - BIPOLAR AMPLIFIER COMPARISON

	CMOS op amp	741 calculated	741 observed
OPEN LOOP GAIN	100 to 100000 (40 - 100 dB)	324000 (110.2 dB)	200000 (106 dB)
INPUT RESISTANCE	essentially infinite	2.7 Mohm	2.0 Mohm
INP. BIAS CURRENT	0.001 pA	38 nA	80 nA
INPUT OFFSET CURRENT	-	3.8 nA	10 nA
INPUT OFFSET VOLTAGE	5 - 15 mV	2.6 mV	2 mV
OUTPUT RESISTANCE	0.1 - 5 kohm for buffered output	47 ohm	75 ohm
PHASE MARGIN	45 - 90 degrees		> than 60 degrees
LOAD IMPEDANCE	1 - 100 kohm 1 - 100 pF		
SLEW RATE	2 - 20 Volt / μsec	0.8 Volt / μsec	0.8 Volt / μsec
FINITE LINEAR RANGE	somewhat smaller than the positive dc voltage	same	same
CMRR	60 - 80 dB		
FREQUENCY RESPONSE	1 - 10 MHz		
NOISE	10 - 50 μVolt RMS		3 - 5 μVolt RMS
POWER SUPPLY REJECTION RATIO	If a power supply voltage contains an incremental component u due to noise then a voltage Ap*u will appear at the output PSRR= (Adifferential gain / Apower) 60 - 80 dB		10 - 150 μVolt / V
DYNAMIC RANGE	The maximum input signal amplitude without generation of excessive nonlinear distortion 30 - 40 dB : open loop 80 - 90 dB : negative feedback with R2/R1=10		
DC POWER DISSIPATION	0.25 - 10 mWatt		50 - 85 μWatt

IV. COMPOSITE OPERATIONAL AMPLIFIERS

A. HISTORY AND FIELD FOR RESEARCH

As stated in previous chapters, the practical OA has several limitations that must be considered in any applications that employ them. In many cases, these characteristics are the limiting factors that prevent improvement in circuit performance. Therefore, the constant need for an improved OA exists, and the composite operational amplifier is a solution that provides many advantages over the single OA.

Composite Operational Amplifiers (CNOAs) were developed by S.N. Michael and W.B. Mikhael in 1981. Their research and its applications have been published in References 1 - 7. Their initial focus and subsequent development of CNOAs, provided a systematic technique for extending the operational frequency range (bandwidth) of linear active networks. Active compensation was examined and applied to the design of active filter networks. The research techniques lead to 136 possible C2OA circuits that were then subjected to the following performance criteria :

(1) The non - inverting and inverting open loop gains of each of the 136 C2OAs should show no change in sign in the denominator polynomial coefficients. This satisfies the necessary but not sufficient conditions for stability.

(2) None of the numerator or denominator coefficients of the non inverting and inverting polynomial coefficients should be realized through differences. This eliminates the need for single OAs with matched GBWPs, and results in low sensitivity of the C2OAs to component variations.

(3) The external three-terminal performance of the C2OA should resemble, as closely as possible, the three-terminal performance of the single OA.

(4) To minimize phase shifts, no right-half s - plane (RHS) zeros due to the single OA pole were allowed in the close loop gains of the C2OAs.

(5) To justify the increased number of OAs, the C2OA had to have an extended frequency operation with minimum gain and phase deviation from the ideal transfer function.[Ref. 8 :pp 7]

After applying the above stringent performance criteria, the 136 designs were tested and four designs were selected that demonstrated superior performance according to the research. Using two OAs each, the four designs were labeled C2OA-1 through C2OA-4 and are shown in Figure 4.1.

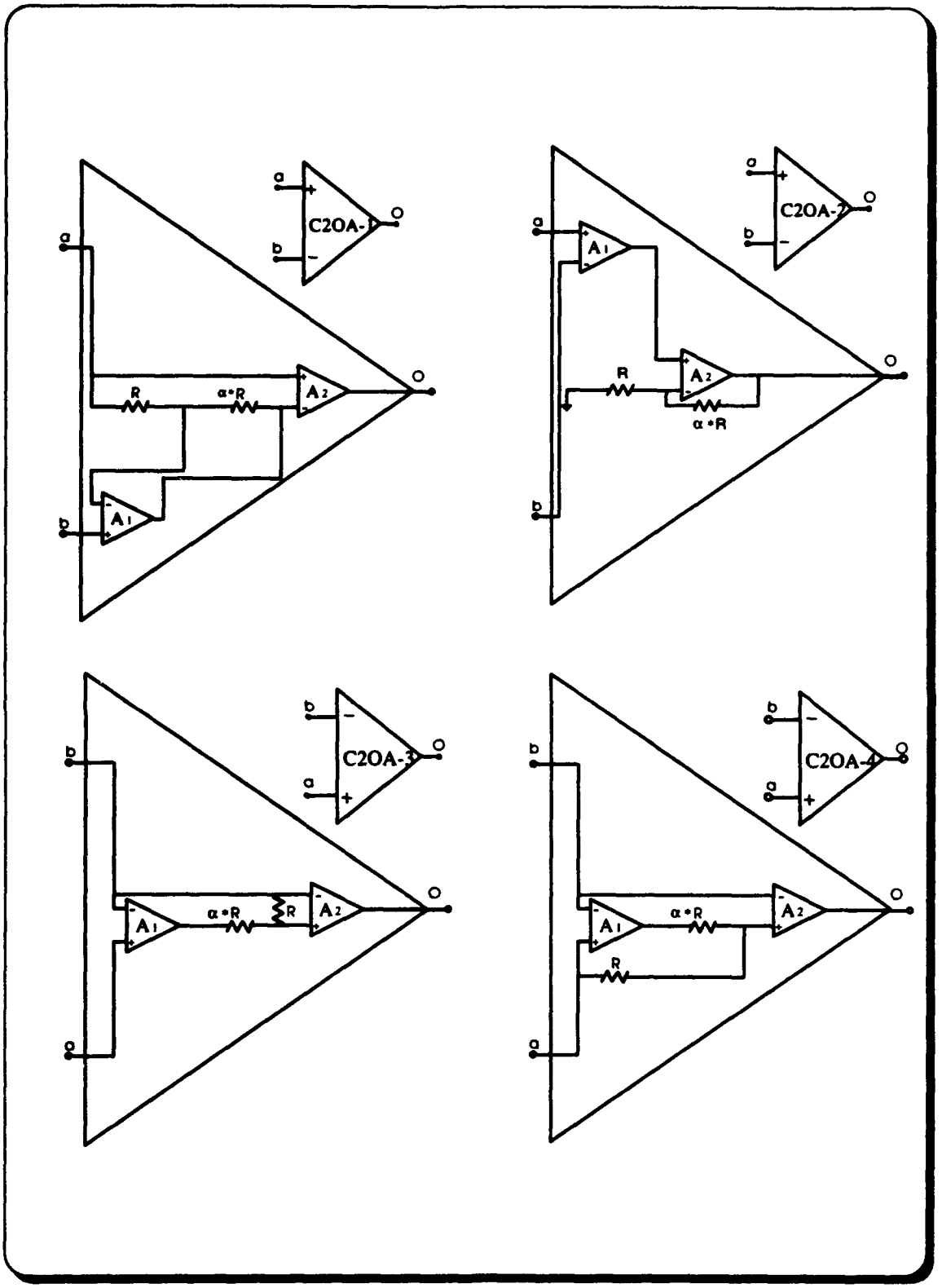


Figure 4.1 The Four CNOAs : C-20A-1, C-20A-2,C-20A-3, and C-20A-4

The present research will be focused on the C2OA-1, in comparison to reference 14 which was focused on the C2OA-2, and will try to give an answer to the problems that were faced in that thesis. It is believed that some of the difficulties found were due to the fact that a theoretical derivation and simulation in the *switched capacitor discrete z-domain* should precede the attempted chip implementation.

The purpose of the present research is to build a third-generation analog-digital VLSI chip, that will prove in the integrated domain, what has so far been tested successfully only using discrete components. Moreover, any of the references 1-7, 8,10,14 written for these composite amplifiers, refers to analysis done in the continuous *s-domain*, which of course is where the origin of the idea was inspired.

As we will see later, because of the VLSI implementation of the composite amplifiers we are obliged to work in the switched capacitor domain, replacing the resistors by capacitors and switches. We cannot base our analysis on the continuous s-domain, and we need to rederive the theoretical behavior of the circuit using sampled data techniques. Thus, it is necessary to derive the new transfer functions in the specially defined *switched capacitor discrete z-domain*, and obtain results similar in performance to those derived in the *s-domain.*

B. THE ANALOG S-DOMAIN THEORY OF THE COMPOSITE OPERATIONAL AMPLIFIER C2OA-1.

An operational amplifier is a voltage controlled voltage source. A model to represent the theoretical infinite input impedance, the zero output impedance, and the infinite open loop gain was needed. This corresponds to the model shown in Figure 4.2, which uses nullator and norator singular elements concept [Ref. 1:pp 450]. A nullator is a one port which neither sustains a voltage, nor passes a current. A norator is a one port which will sustain an arbitrary voltage and pass an arbitrary independent current. It is represented by the *nullor chain transmission matrix*, described in the following equation :

$$\begin{bmatrix} V1 \\ I1 \end{bmatrix} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} * \begin{bmatrix} V2 \\ -I2 \end{bmatrix} \qquad (4.1)$$

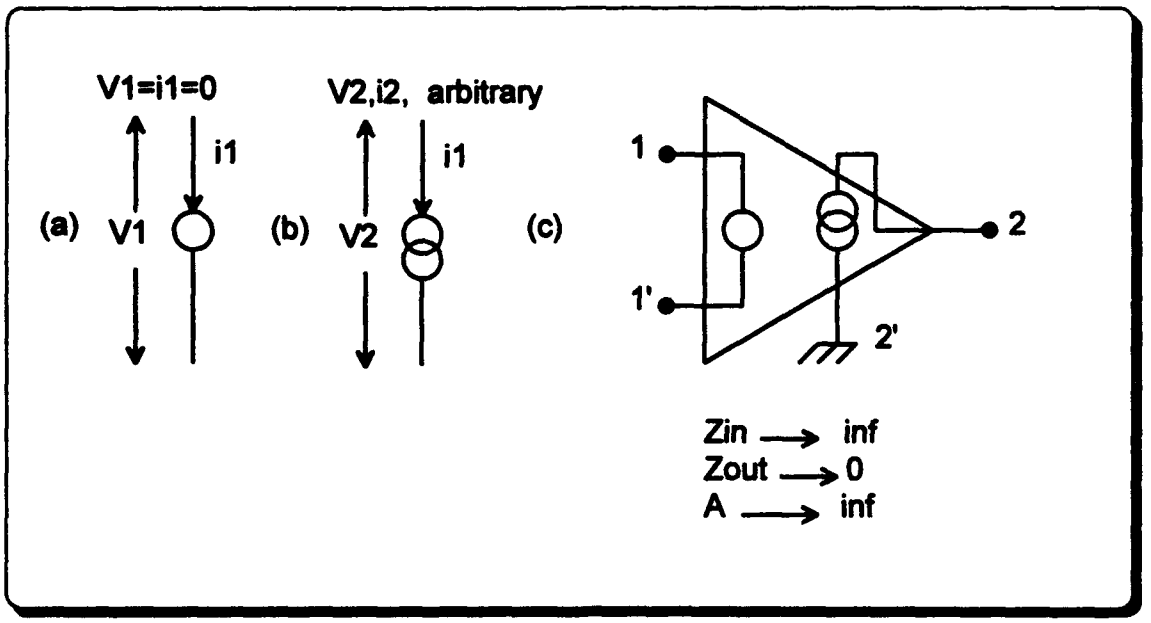


Figure 4.2 (a) Nullator , (b) Norator, (c) Nullor Representation

The open - loop gain of the single OAs used in modeling the C2OAs (assuming a single pole model) is

$$A_i = \frac{A_{oi} * \omega_{Ui}}{\omega_{Ui} + s} = \frac{\omega_i}{s + \omega_{Ui}} \quad , \quad i = 1,2 \qquad (4.2)$$

where A_{oi} , ω_{Ui} , and ω_i are the dc open - loop gain, the 3-dB bandwidth, and the GBWP of the i-th single OA, respectively. The open-loop input output relationships for the four composite amplifiers C2OA-i are given by

$$V_{oi} = V_a * A_{ai}(s) - V_b * A_{bi}(s), \; i = 1,2,3,4 \qquad (4.3)$$

Here the subscript a represents the positive input terminal and b the negative input. Applying Kirchoff's laws to the open loop circuit of Figure 4.2, the equations of Table 4.1 can be derived. In Table 4.1, k represents the ratio of the external resistors used to produce the negative or positive feedback, respectively. On the other hand, α is the ratio of the internal resistors used, as shown in Figure 4.1, and is critical for the position of the poles of the amplifier. Upon examining the stability condition described by equation 4.10, one finds that α imposed is physically realizable for all k. In practice, α should be chosen in the stable range, for a given k, that results in the best realizable value of Q_p and ω_p. We also observe that as ω_p increases for a fixed Q_p, both amplitude and phase deviations of T_a from T_i, at a given frequency ω (where $\omega < \omega_p$), decrease.

TABLE 4.1 EVALUATION RELATIONSHIPS FOR THE COMPOSITE AMPLIFIER C-2OA-1

Open loop transfer function	$V_{o1} = V_a * \frac{A_2*(1+A_1)*(1+\alpha)}{A_1+(1+\alpha)} - V_b * \frac{A_1*A_2*(1+\alpha)}{A_1+(1+\alpha)}$	(4.4)
Single ended inverting : Va = 0	$A_{oC1} = \frac{A_o*(1+\alpha)}{1+\frac{1+\alpha}{Ao}} \approx A_o * (1+\alpha) \;\; : (1+\alpha) < A_o$	(4.5)
Negative finite gain transfer function	$T_a = T_{ideal} * \frac{1}{1+(\frac{s}{\omega_p*Q_p})+(\frac{s^2}{\omega_p^2})}$	(4.6)
Positive finite gain transfer function	$T_a = T_{ideal} * \frac{1+\frac{s}{\omega_1}}{1+(\frac{s}{\omega_p*Q_p})+(\frac{s^2}{\omega_p^2})}$	(4.7)
3 dB bandwidth equation	$\omega_p = \sqrt{\frac{\omega_1*\omega_2}{1+k}}$	(4.8)
Quality factor	$Q_p = \frac{(1+\alpha)}{\sqrt{1+k}} * \sqrt{\frac{\omega_1}{\omega_2}}$	(4.9)
Routh - Hurwitz stability criterion	$(1+\alpha) < \frac{1+k}{2}$	(4.10)
Common mode rejection ratio	$CMRR = A_{o1} + 0.5$	(4.11)
CONCLUSIONS	a) The composite amplifier has a single pole rolloff from ω_i / A_o to $\omega_i / (1+A)$, where the second pole occurs. As the ratio α increases, the dc gain increases, while the frequency of the second pole decreases. b) The voltage swing at the first OA output is always less than the output voltage V_o. Consequently, no dynamic range reduction of V_o or harmonic distortion problems should arise. c) A mismatch of + or - 5 % in ω_1 and ω_2 results in a + or - 5 % change in ω_p and a + or - 2.5 % change in Q_p Therefore the mismatched GBWPs within practical ranges can be used without appreciably affecting the stability or the sensitivity of the finite gain realizations.	

C. COMPARISONS USING THE C-2OA-1

1. The STC circuits, classification

Single-time-constant (STC) circuits are those circuits that are composed of, or can be reduced to, one reactive component (inductance or capacitance) and one resistance. An STC circuit formed of an L and a R has a time constant $\tau = L / R$ another One formed of an R and a C has $\tau = C * R$. Although STC circuits are quite simple, they play an important role in the design and analysis of linear and digital circuits. For instance, the analysis of an amplifier circuit can usually be reduced to the analysis of one or more STC circuits.

STC circuits can be classified into two categories, low pass (LP) and high pass (HP) types, with each of the two categories displaying distinctly different signal responses. The task of finding the type of a circuit is easily accomplished by examining its frequency response. Specifically, low pass circuits pass dc and attenuate high frequencies, with the transmission being zero at ω=infinity. The Table 4.2 provides the rules to classify the behavior of STC circuits.

Due to the existence of a low frequency pole, all OAs have an equivalence of low pass circuits. Their difference is mainly how broad and flat will their useful bandwidth be, before reaching the 3 dB attenuation. The transfer function T (s) of an STC low-pass circuit of one pole model

like the 741 OA can always be written in the form

$$T(s) = \frac{k}{1+\frac{s}{\omega_0}} \tag{4.12}$$

which for physical frequencies , where s=j*ω becomes

$$T(s) = \frac{k}{1+j*(\frac{\omega}{\omega_0})} \tag{4.13}$$

where k is the magnitude of the transfer function at $\omega = 0$ (dc) and ω_0 is defined by

$$\omega_0 = 1 / \tau \tag{4.14}$$

with τ being the time constant. Thus, the magnitude response is given by

$$|T(j*\omega)| = \frac{k}{\sqrt{1+(\frac{\omega}{\omega_0})^2}} \tag{4.15}$$

and the phase response is given by

$$\phi(\omega) = -\tan^{-1}(\frac{\omega}{\omega_0}) \tag{4.16}$$

At $\omega = \omega_0$, as one can calculate from these relationships, the gain drops by a factor of $\sqrt{2}$ relative to the dc gain, which corresponds to a 3 - dB reduction of gain. The ω_0 corner frequency is appropriately referred to as the 3 - dB frequency [Ref. 19 : pp E-1].

TABLE 4.2 CLASSIFICATION RULES FOR STC CIRCUITS

Test at	Replace	It is LP if	It is HP if
ω=0	C by open circuit L by short circuit	Output is finite	Output is zero
ω=inf	C by short circuit L by open circuit	Output is zero	Output is finite

2. Increased bandwidth and better sensitivity

The single OA, when used in a finite-gain amplifier configuration, has a bandwidth that decreases approximately by a factor of 1/k, relative to its gain-bandwidth product (GBWP).

It is interesting to see what happens when two OAs are cascaded together in a finite-gain amplifier configuration. The maximally flat GBWP, which is the optimum result, is obtained when each OA (A1 and A2) has an individual gain of $k^{0.5}$, in order to realize an overall gain of k. The resulting bandwidth shrinks by approximately $0.66*k^{0.5}$. The GBWP of C2OA-1, in comparison, can be designed to shrink by only a factor of $k^{-0.5}$ for Q_p = 0.707 (maximally flat) [Ref. 4 and 8]. These theoretical BW's are shown more clearly in Figure 4.3.

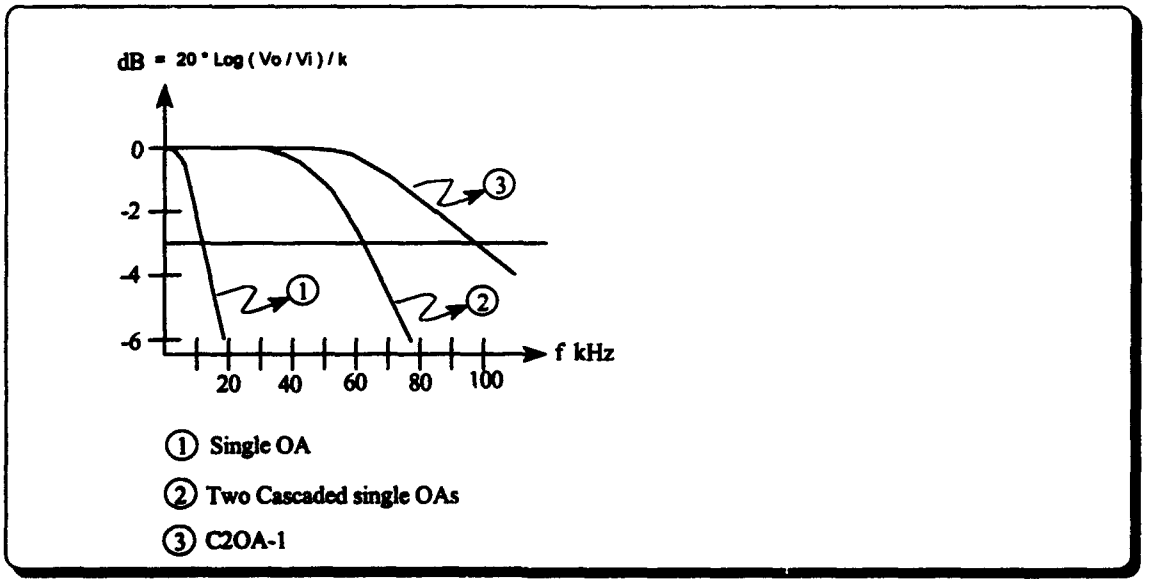


Figure 4.3 Comparisons of Frequency Responses for Different Negative Finite Gain Amplifiers (Gain Applied = -100, GBWP = 1 MHz)

As far as the sensitivity is concerned, as we have seen from the Table 4.1, the finite gain transfer functions for the C2OAs have the general form

$$GF = \frac{1+a*s}{1+b_1*s+b_2*s^2} \quad : b_1 = \frac{1}{\omega_p * Q} \quad , \quad b_2 = \frac{1}{\omega_p^2} \quad , \qquad (4.17)$$

Neither the *a* nor *b* coefficients are realized through differences, thus eliminating the need for single OAs with matched GBWPs and results in low sensitivity of the C2OA with respect to its components. [Refs. 3,4]

3. Lower I/O offset voltages and higher slew rate

The small dc voltage differential at the inputs of an OA, that is needed to null the output, is referred to as the input offset voltage (V_{off}). This voltage, when amplified by the gain of the amplifier, is referred to as output offset voltage. This differential input can be attributed to a voltage difference applied to the two inputs of the OA, or to a voltage difference due to a mismatched transistor pair in the input differential stage having different gains and different internal impedances, or both.

The smaller the offset voltage, the more accurately the OA can detect and amplify the input signal. This small differential voltage, when amplified, could produce a large error in the output signal. The most common solution to this problem is to use an input bias resistor, or to select an OA with a smaller offset voltage. The first solution is not always practical because not all designs allow for an input bias resistor to be used,

which may lower the slew rate. The composite OA allows for yet another solution, select a small offset voltage OA for A_1 and select a high slew rate OA for A_2. The value of the input offset voltage for the composite amplifier C2OA-1, V_{off} is given from the equation

$$V_{off} = V_{off1} + (\frac{V_{off2}}{\alpha}) \qquad (4.18)$$

One can notice that V_{off} is, for all practical purposes, a function of V_{off1} alone and not of V_{off2}. As long as α remains relatively large, V_{off2} will not play a substantial part in the overall value of V_{off}.[Ref. 8 : pp 22]

As far as the slew rate is concerned, it is dependent upon the bias current and the internal compensation capacitor value. A faster slew rate is preferable in most applications. However, a faster slew rate comes at the expense of an increase in input offset voltage. Most OA designs either incorporate a fast SR design or they incorporate a small offset voltage design.

Alternatively, the composite OA offers another solution. As shown earlier, the offset voltage is mostly determined by the A_1 op amp. Thus, one can choose the input OA with a very small offset voltage along with its distortion and dynamic range limitations. This will not hinder the output of the composite OA due to the composite's output being dependent upon the characteristics of the output op amp A_2.[Refs. 1,2,8] The A_2 OA can be chosen for its high slew rate, wide bandwidth, and fast settling time,

a high slew rate, wide bandwidth, fast settling output stage for superior performance. The alternatives rely on the careful selection of the internal amplifiers A_1 and A_2. Thus, at the end of this chapter, we can understand the importance that was given in the previous chapters to enhance the knowledge of single bipolar and CMOS OAs, since they are alternatively the main building block of the composite amplifier C-2OA-1.

V. SWITCHED CAPACITOR NETWORKS

A. THE NEED FOR SWITCHED CAPACITOR NETWORKS

Any electronic circuit discussed so far included some resistance necessary for various reasons, such as biasing an amplifier, creating feedback, etc. It is also known that the time constant of a circuit, including resistors and capacitors, is equivalent to R * C. Since resistors and capacitors are made at different steps in the fabrication process, their errors do not track one another. In addition, the temperature and voltage coefficients of resistors and capacitors are not correlated. Therefore, time constants will vary with temperature and signal level. The solution is to make the time constant a factor depending only on one parameter and not two. This is accomplished by replacing the resistors in the circuit with switched capacitors. Equation 5.1 is the governing principle by which the substitution is done, because it represents an approximation of the resistance that the capacitor is replacing

$$R = \frac{1}{f_c * C_R} \tag{5.1}$$

where f_c is the frequency of the clock used to switch the capacitor and C_R is the value of the capacitor that replaces the resistor. The circuit or network that replaces the resistor and satisfies this expression, is called the switched capacitor (SC) and is shown in Figure 5.1.

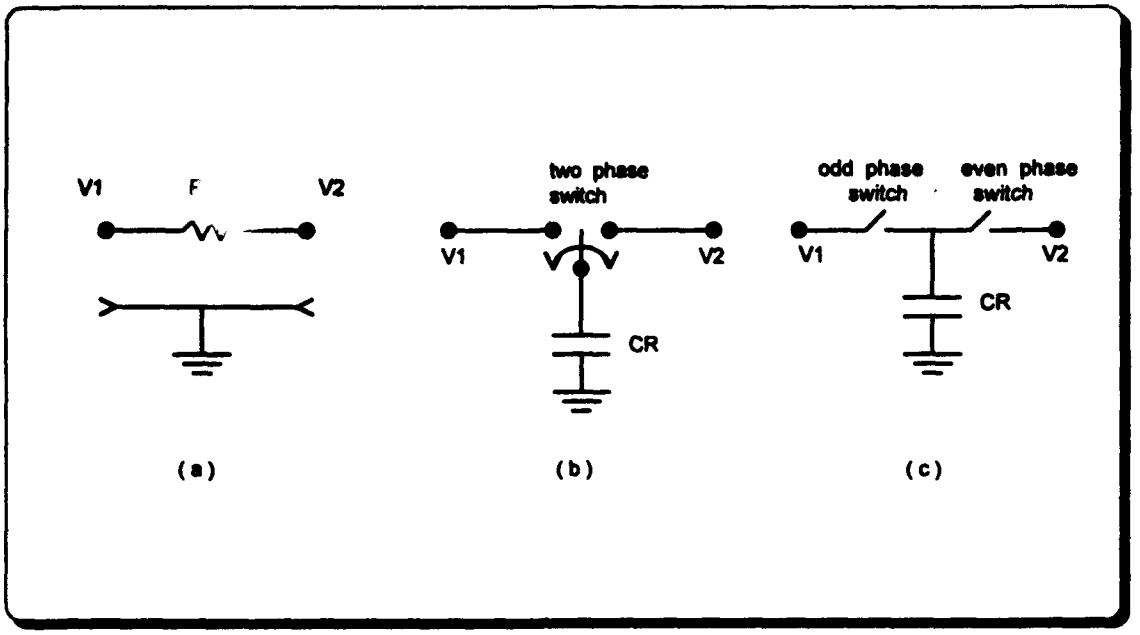


Figure 5.1 (a) Resistor, (b) Switched Capacitor Equivalent, (c) Circuit Diagram

It has been shown in detail, in reference 8, that with proper clock frequency and phase a network of switched capacitors can emulate the operation and performance of a resistor in a circuit. In Figure 5.1 (c) two non-overlapping clock signals, Φ_o and Φ_e, are used to ensure that the capacitor is in fact switched between the two voltages without any possibility of both switches being closed at the same time. The two clock signals are generated from a single clock for synchronization. The new time constant τ_0 is vulnerable only to capacitance values and frequency

$$\tau_0 = 1/\omega_0 = C/(f_c * C_R) \qquad (5.2)$$

B. POSITIVE RELATIONSHIP BETWEEN SWITCHED CAPACITOR NETWORKS AND MOS TECHNOLOGY.

1. Overview to all applications

A property unique to MOS integrated circuits is the ability to store charge on a node for several milliseconds and to sense this stored charge continuously and non-destructively. This storage in MOS integrated circuits comes about naturally and cheaply. Recently, it has been found more attractive to implement MOS analog sampled-data filters as active switched capacitor filters. SC filters are recursive or infinite impulse response (IIR) filters. Therefore, high Q's and flat passbands can be realized efficiently. Furthermore, sampling rates in excess of 100 KHz can be routinely used. The use of high sampling rates serves to lessen the burden placed on the continuous anti-aliasing filter which must band-limit the input spectrum to one-half the sampling frequency. We must note that sufficient anti-aliasing can usually be achieved with a relatively imprecise second-order continuous active filter. These are some of the features that render switched capacitor filters more attractive implementations than CCD filters for many applications.

In addition, SC filters take full advantage of the inherent precision achieved by MOS processing. As will be seen later, the transfer function coefficients are completely determined by a single, precise crystal-

controlled clock frequency and ratioed capacitors. It has been shown that capacitor ratios can be held to accuracy of about 0.1 %, and with appropriate VLSI techniques, capacitance as small as 0.1 pFarad can be used. Furthermore, MOS capacitors are nearly ideal, with very low dissipation factors and good temperature stability. Of economical importance, precision SC circuits can be fabricated using memory-like NMOS and CMOS processing. Thus, analog and digital circuitry can be placed on the same chip, providing the capability of integrating complete systems on a single chip [Ref. 13: pp 377].

Of course, the more striking advantage that "engages" CMOS technology with switched capacitor networks is the drastical reduction of the required "real estate" on an integrated circuit. To give us some idea as to how much area can be saved, let's assume that C_R was 1 pF. Using equation (5.1) and a nominal frequency of 100 KHz results in an R value of 10 MΩ. The 1 pF capacitor will occupy a chip area of approximately 2500 μm^2, and the 10 MΩ resistor will occupy a chip area of approximately 10^6 μm^2. Thus, the capacitor requires only a chip area of about 0.25 % the area of the resistor it replaces.

2. Logical connection with operational amplifiers : A first specific application as an example

The performance objectives for operational amplifiers to be used within a monolithic analog subsystem are often quite different from those of stand-alone amplifiers. Perhaps the most important difference is the fact that for many of the amplifiers in the system, the load that the amplifier has to drive is well defined and is often purely capacitive with values of a few picofarads. In contrast, stand-alone general purpose amplifiers usually must be designed to achieve a certain level of performance that is independent of loading over capacitive loads of up to several hundred picofarads and resistive loads down to 2 KΩ or less. Within a monolithic analog subsystem, only a few of the amplifiers must drive a signal off-chip where the capacitive and resistive loads are significant and variable. These amplifiers will be termed *output buffers*, and the amplifiers whose outputs are not driving external nodes will be termed *internal amplifiers*.

A typical application of an internal operational amplifier, a switched capacitor integrator, is illustrated in its simplest form in Figure 2.2. This circuit is widely utilized as the basic element of monolithic switched-capacitor filters, primarily because the frequency response of the integrator is insensitive to the various parasitic capacitance that are present on both terminals of the monolithic capacitors that are used in the circuit.

The integrator consists of an operational amplifier, an integrating capacitor Ci, a sampling capacitor Cs , and four MOS transistor switches that

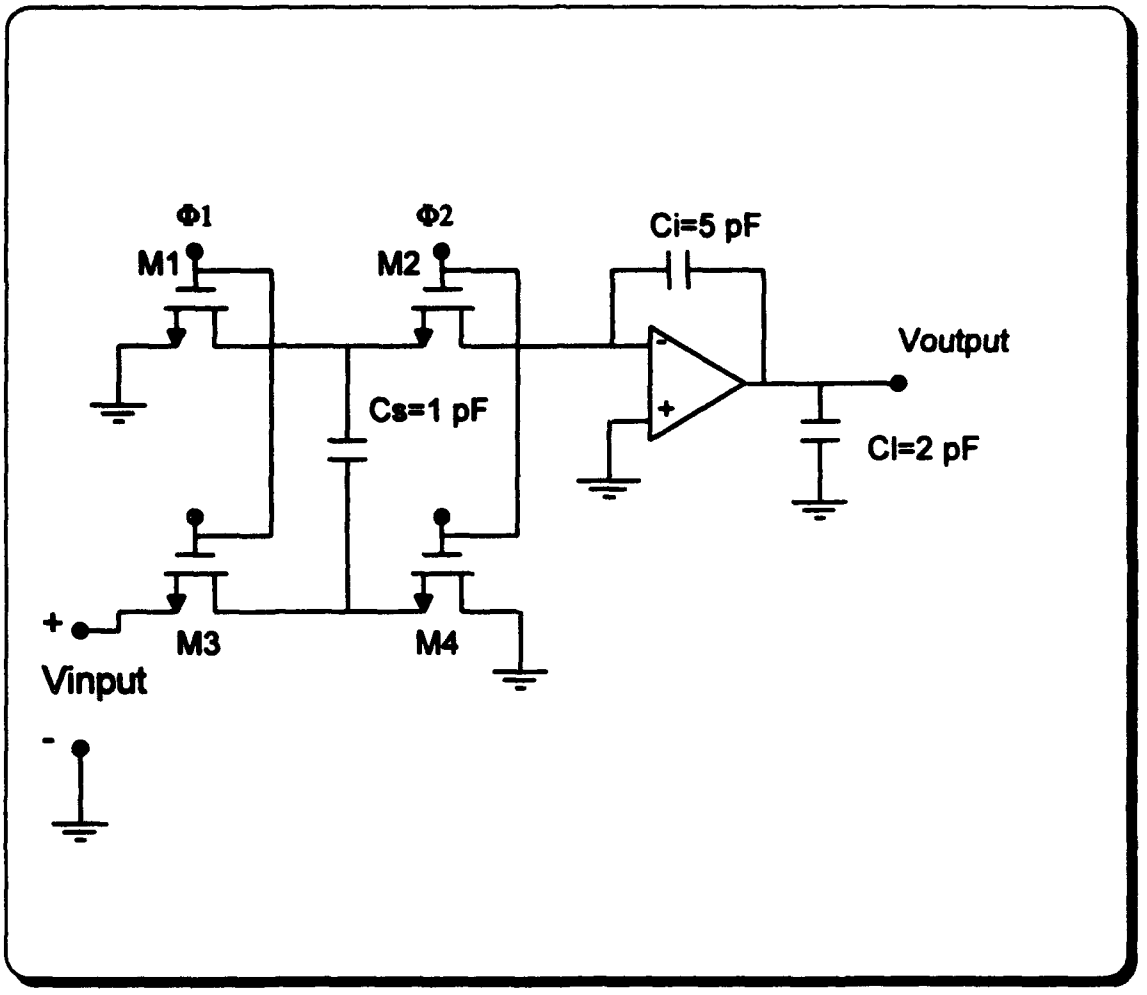


Figure 5.2 A Switched Capacitor Integrator

are driven by clock signals. A key requirement for the operational amplifier is that dc currents at its input terminals must be extremely small in order to not lose any of the charge on the switched capacitors. This application is thus ideally suited to op amps using MOS transistors in the input stage. Hence, we can understand why the switched capacitor networks require the use of CMOS operational amplifiers which have already been introduced in chapter 3.

C. COMPARISON OF SWITCHED CAPACITOR APPLICATIONS VERSUS DIGITAL IMPLEMENTATION

1. Non-ideal properties of switched capacitors

As we have already seen, the switched capacitor equivalent model contains switches. These switches, when clocked, will produce the following undesirable side effects, which are analyzed in more detail in Reference 8.

a. Clock feed through

Though the clocks used in switched capacitor networks are not a part of the signal itself, the switches that produce the two phase non-overlapping clocks, Φ_{odd} and Φ_{even} use the gate-to-source and the gate-to-drain paths of the MOS capacitor to introduce clock feed through into the circuit which causes signal contamination. We can minimize its effect by maximizing the size of the unswitched feedback capacitor.

b. Offset Voltage error and Noise

This has been discussed in chapter 2.

c. Nonlinear PN junction capacitance

It is otherwise called internal (stray) parasitic capacitance. It is unpredictable and can significally affect the performance of any switched capacitor network. It cannot be eliminated, but its results can be nullified by choosing the appropriate switched capacitor topology. This is very important because one can identify all the possible combinations of parasitic

capacitances and adopt a symmetrical stray insensitive design before trying to implement the circuit on a chip. One common method to nullify the effects of bottom plate parasitic capacitance is to connect the bottom plate of C_R to ground, to an independent voltage source, or to an OA output. This connection will reduce the accumulated parasitic capacitance at the OA virtual ground. The rules to eliminate the parasitic capacitance can be summarized as follows :

(1) Capacitors between the inverting input of the OA and the switch are at virtual ground and thus always shorted.

(2) Capacitance driven by a voltage source is zeroed.

(3) Capacitance between the output of an OA and ground is zeroed (since the OA resembles an ideal voltage source).

d. Incomplete transfer of charge

Using discrete component implementation, it is not unusual to have leaky capacitors, but in integrated circuit implementations capacitor leakage is usually very small.

2. Disadvantages

(1) **Limited accuracy :** So far, switched capacitor networks are built to within a 0.1 % tolerance of their nominal values, which is much better than the minimum 20 % tolerance of an integrated resistor, but still open to improvement.

(2) **Limited dynamic range :** The extended use of OAs and switches introduce additional noise apart from the noise introduced by supply lines and the clock. This would result in a dynamic range of 70 to 100 dB. Digital signal processors maintain a much higher dynamic range.

(3) **Flexibility and programmability :** The SC circuits can be made to be programmable, however the digital domain is much easier in that case. The best solution is that the programmability part is accomplished by a digital circuit in cooperation with the SC one.

(4) **Enormous evolution in microprocessor technology:** The speed is constantly increasing and the DSP performance becomes constantly better.

3. Advantages

A question one may ask is why someone would prefer to deal with switched capacitor and analog networks since there are so many difficulties. The answer is simple, there are some advantages that cannot be surpassed by digital technology. A purely digital system will always require an A/D converter that has speed limitations. Thus, the system can never produce real time results. Also, there are some applications, like neural networks and artificial intelligence, that constantly become more complicated

and their results need an enormous number of calculations if they are to be done by digital circuits. On the other hand, these functions can be naturally performed using much simpler analog networks. Thus, implementation of these networks would be simpler, faster, and would require a limited IC real estate and small dc bias power. Also, whenever we have cases where the input or output signals are inherently analog in nature, then switched capacitor implementation would be the preferred choice for implementation.

More than this, as we saw in the case of composite amplifiers, the integration in the same chip of the analog and digital technology is an effort to combine the individual advantages of both technologies in order to improve the overall product.

VI. THEORETICAL FOUNDATION OF THE STRAY INSENSITIVE SWITCHED CAPACITOR IMPLEMENTATION OF THE COMPOSITE AMPLIFIER C-2OA-1

A. OVERVIEW OF THE COMPOSITE OA AS AN IDEAL SC NETWORK

1. Rules of operation

An ideal SC network is comprised of ideal capacitors, ideal switches, and ideal voltage-controlled voltage sources (i.e., infinite, frequency independent gain, or infinite-gain bandwidth operation amplifiers) when excited by sampled-data voltage inputs. It is noted that MOS op amps have been designed which settle to within 0.1 % of final value in 2μsec and achieve dc gains greater than 60 dB. Therefore, for sampling rates of less than 250 KHz, a good approximation of an actual MOS op amp is a voltage controlled voltage source with gain of A_0. Typically, the switches are controlled by a two-phase, non-overlapping clock of frequency $f_c = 0.5 * T$. We use ϕ^{even} to denote the even clock phase, which instantaneously closes the *"e"* switch on the even $2 * n * T$ times. Similarly, ϕ^{odd} denotes the odd clock phase, which instantaneously closes the *"o"* switch on the odd $(2*n+1)*T$ times. The switches are assumed to have a 50 % duty cycle with equal (T second) on and off time periods.The upper and lower limits on clock frequency are usually dictated by the settling time of the operational amplifier

and various other requirements (e.g. noise, capacitor leakage, Nyquist rate, and anti-aliasing specifications). Clock rates up to 1 MHz seem feasible. As indicated in reference 13, as the clock rate increases, the capacitor ratios also increase, hence the silicon area, increases. Therefore, in practice, the clock rate is typically chosen no higher than is required to achieve the desired degree of anti-aliasing protection with a second-order continuous filter of sufficiently high cutoff frequency to render its main passband variation acceptably small. The behavior of switched capacitor filters is strongly dependent on the clock period and typically is insensitive to the duty cycle (or it can be made to be so).

2. Rules of analysis

a. Concepts, assumptions, techniques and their relationship with z-transform.

Along with the form of the clocks, it will be further assumed that both the input and output of the SC network are sampled-data signals which change in value only at the switching instants k * T. Thus, in their more general form, the voltage sources and internal circuit voltages are assumed to be sampled at times k * T and held over a one-half clock period interval T as shown in Figure 6.1. With this assumption, we can apply z-transform techniques to the general synthesis and analysis of SC networks. The z-transform $z = e^{s*tau}$,where s is the complex analog frequency

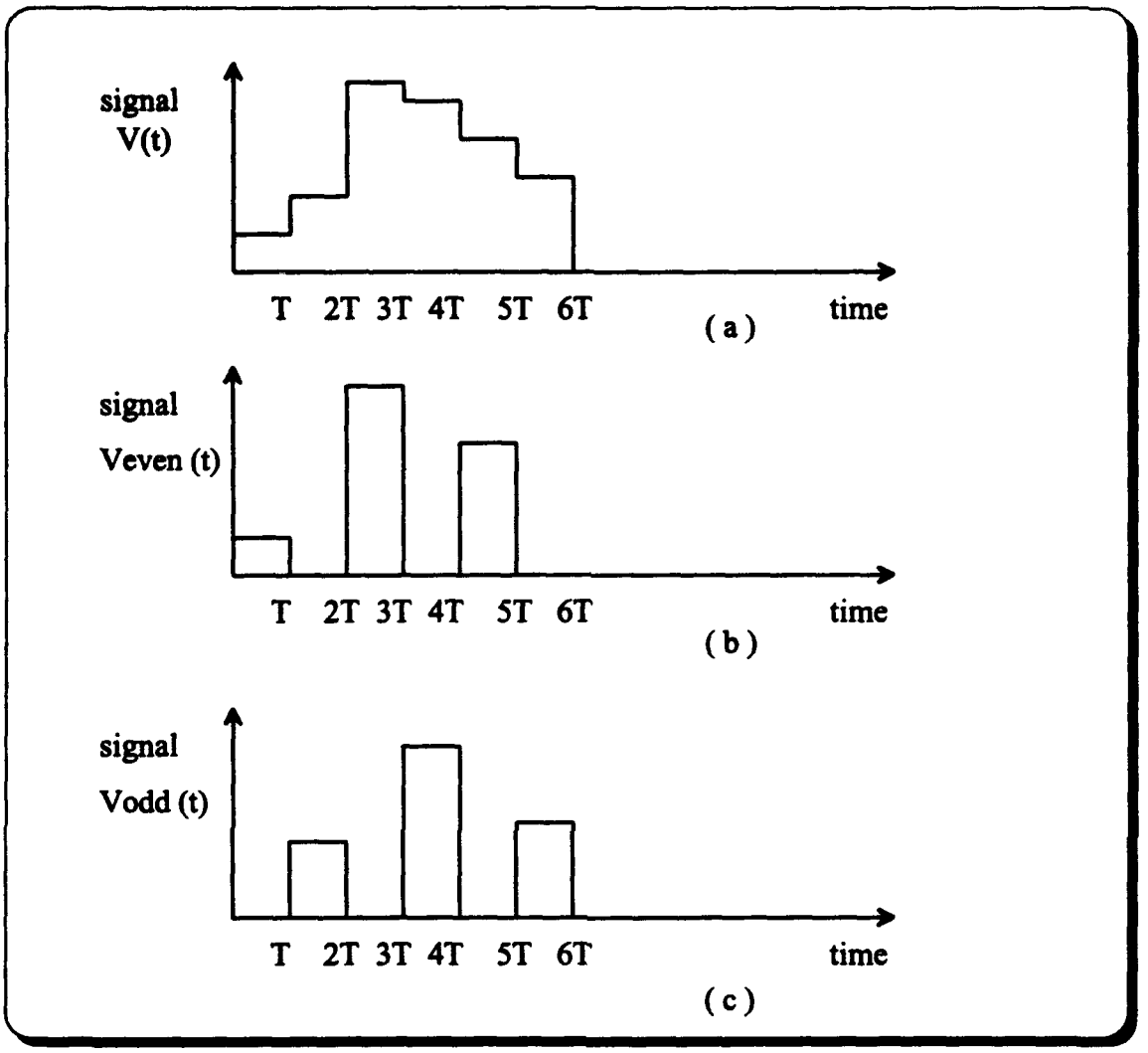


Figure 6.1 Sampled-Data Voltage Waveforms

variable and $\tau\alpha\upsilon = 2*T$ the clock period, then provides us with a convenient means for performing frequency domain analysis. Whenever there might be some unusual numerators or denominators with exponents in partial powers of z, we will solve this problem by simply redefining the z- transform according to

$$\hat{z} = e^{s*\frac{T}{2}} \tag{6.1}$$

This means that by doubling the effective sampling rate, and instead of working in the z-domain one would be working in the newly defined $\hat{z}$

domain. To restore the analog character to the z-transform-computed frequency response, this response must be modified by a multiplicative : $\frac{\sin(\omega*\frac{\tau}{2})}{\omega*\frac{\tau}{2}}$, where τ is the sampling period. For high sampling rates where $\omega * \tau << 1$, the passband of the frequency response is left virtually unaffected.

One can view the time varying SC network, with biphase switches, as two interrelated time-invariant networks. In view of this fundamental approach, it is mathematically convenient to partition the sampled-data waveform into its even and odd components. This observation opened the door to a rigorous understanding of switched capacitor networks and resulted in several methods for their analysis. One way to interpret the relationship between the even and odd topologies is to consider them topologically decoupled, with the states of one determining the initial conditions for the other. This interpretation results in two distinct circuits coupled together via dependent sources which establish the aforementioned initial conditions. Of course, this step must be composed into a single z-domain equivalent circuit. In general, an n-port bi-phase SC network will require a 2*n-port equivalent circuit, (i.e., n-ports for the even clock phase and n-ports for the odd clock phase). It is this interpretation that provides the kinds of valuable insight that Laplace transform techniques have provided for linear time-invariant networks.

b. Conservation of energy : A leading principle

Since SC networks can be most rigorously characterized in terms of charge-transfer operations, discrete-time voltages u_i (kT) and discrete time charge variations or transfers Δq_i (kT) are used as port variables. At the switching times kT, charges are instantaneously redistributed, with the principle of charge conservation maintained at every node in the network. Due to the biphase switching operation, two distinct, but coupled nodal charge equations are required to characterize the charge conservation condition at a particular node for all the real time instants kT,(where T odd or even).

$$\Delta q_p^e(k*T) = \sum_{i=1}^{M_{ep}} *q_{pi}^e(k*T) - \sum_{i=1}^{M_{ep}} * q_{pi}^o[(k-1)*T] \; : k = even \; int. \quad (6.2)$$

$$\Delta q_p^e(k*T) = \sum_{i=1}^{M_{op}} *q_{pi}^o(k*T) - \sum_{i=1}^{M_{op}} * q_{pi}^e[(k-1)*T] \; : k = odd \; int. \quad (6.3)$$

or equivalently in the z-domain

$$\Delta Q_p^e(z) = \sum_{i=1}^{M_{ep}} Q_{pi}^e(z) - z^{-\frac{1}{2}} * \sum_{i=1}^{M_{ep}} Q_{pi}^o(z) \quad (6.4)$$

$$\Delta Q_p^o(z) = \sum_{i=1}^{M_{op}} Q_{pi}^o(z) - z^{-\frac{1}{2}} * \sum_{i=1}^{M_{op}} Q_{pi}^e(z) \quad (6.5)$$

where q_{pi}^e , q_{pi}^o and Q_{pi}^e , Q_{pi}^o denote, respectively, the instantaneous charges stored on the ith capacitor connected to node p for the even and odd kT time constants and their z-transforms. Also, M_{ep} and M_{op} denote respectively, the total number of capacitors connected to node p during the even and odd clock phases. When the charge is sensed during the even clock phase, q_{pi}^e (kT) represent the charges that reside on the capacitors C_{pi} at a particular even kT instant of time and also the

q_{pi}°[(k-1)*T] serve as the initial condition for circuit action observed at this even time instant. An analogous description can be given for charge during the odd clock phase.

For single capacitor SC blocks, z-transformed nodal charge equations lead directly to simple z-domain equivalent circuits. It is exactly this approach that this investigation will follow in order to analyze the composite amplifier C2OA-1. The equivalent circuits impose a graphical transformation in the original circuit, and then we need to apply Kirchoff's rules in the new circuit in order to derive the transfer function.

B. STRAY INSENSITIVE REALIZATION OF THE SC C2OA - 1 : HARDWARE DESCRIPTION

It has already been mentioned that the only way to eliminate the effects of stray capacitance is through an appropriate design. It has been proven in reference 8 that there are two SC topologies which when they replace the resistors in the C-2OA-1 design, make the resultant SC network stray insensitive. This investigation agrees with the proof of reference 8, but corrects for the right name of the two SC topologies used. Their correct names are toggle switched inverter (TSI) - instead of toggle switched capacitor (TSC) as it is mentioned in reference 8 - and modified open-circuit floating resistor (MOFR) and are shown in Figures 6.3 and 6.4

along with the composite OA C2OA-1 which is shown in Figure 6.2. The α in the capacitor indicates that there is a ratio between the two capacitors. The reader is prompted to reference 13, page 403, to check for the exactness of this correction. As we will see later this name difference is important to the quality of feedback that is implied, and accordingly to the stability of the system.

An important remark that came after the implementation of the theory into a discrete circuit (on a bread board), is the need of a feedback capacitor Cn, even if this is not included in the replacement of the resistors from switched capacitors. Its use, as it will be verified from simulations with and without it, is to maintain the continuity of the output signal, which otherwise is affected by the time gaps between the even and odd switching. Th' would prevent the CMOS amplifier A1 from being in an open loop configuration for a short period of time and would have caused it to become unstable, producing a distorted output. A small feedback capacitor of a value such as 10 picofarads would succeed in preventing A1 from being in an open loop situation, thus giving the expected stable operation and smooth output. The value of this capacitor had been introduced experimentally in reference 8 and verified from simulations in this investigation, and cannot be less than 5 picofarads.

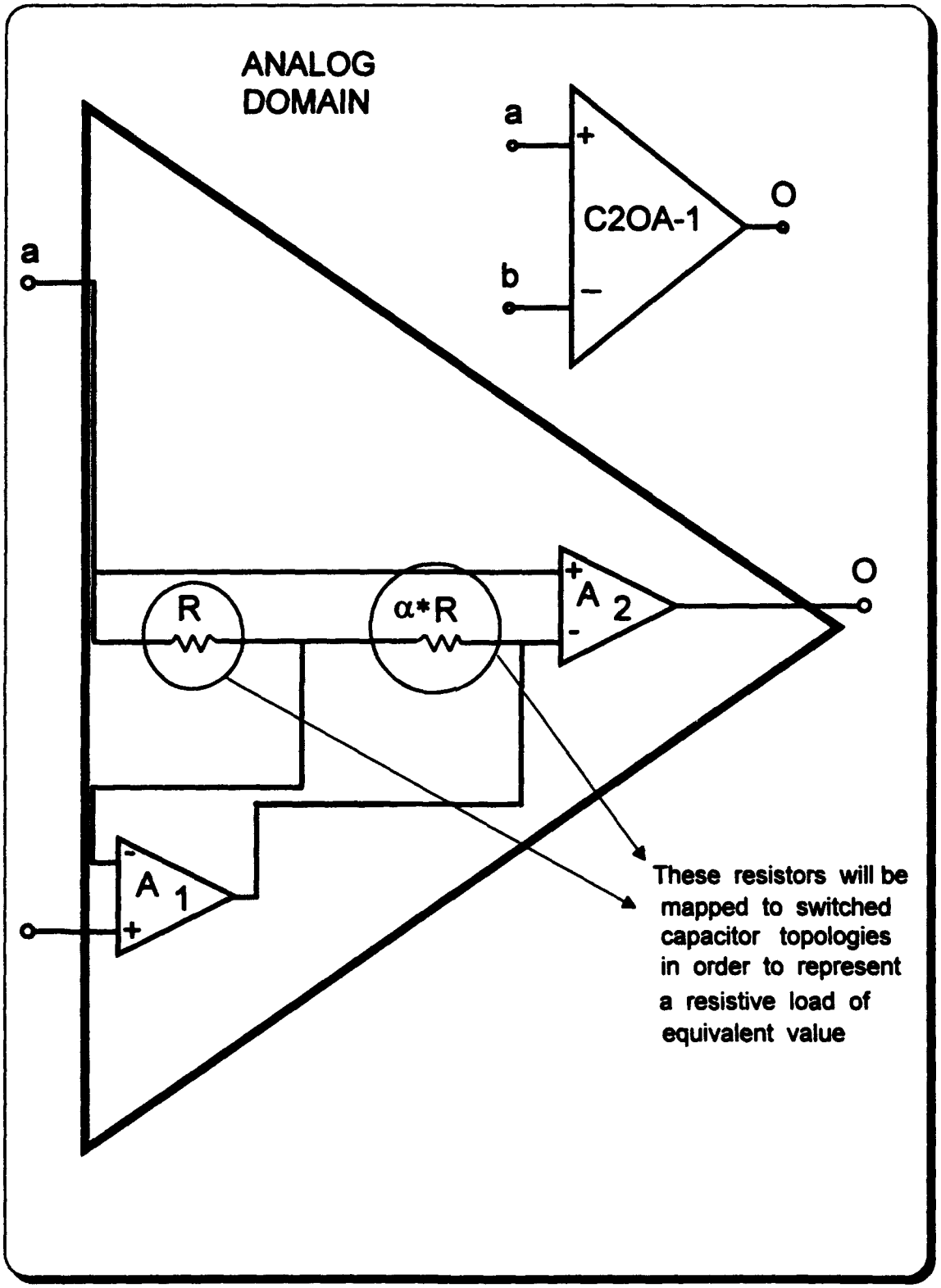


Figure 6.2 Composite Amplifier C2OA-1

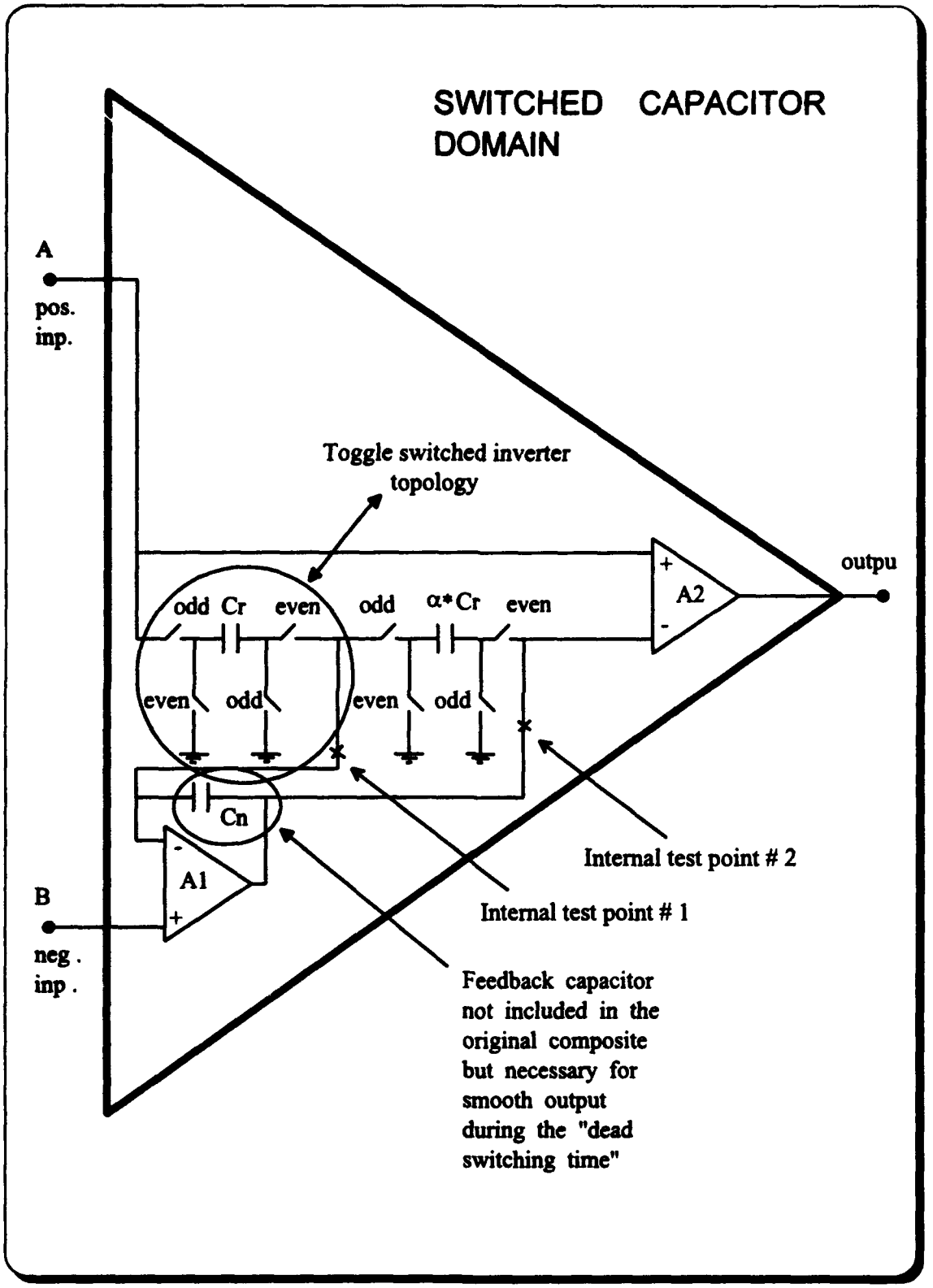


Figure 6.3 Stray Insensitive TSI C2OA-1

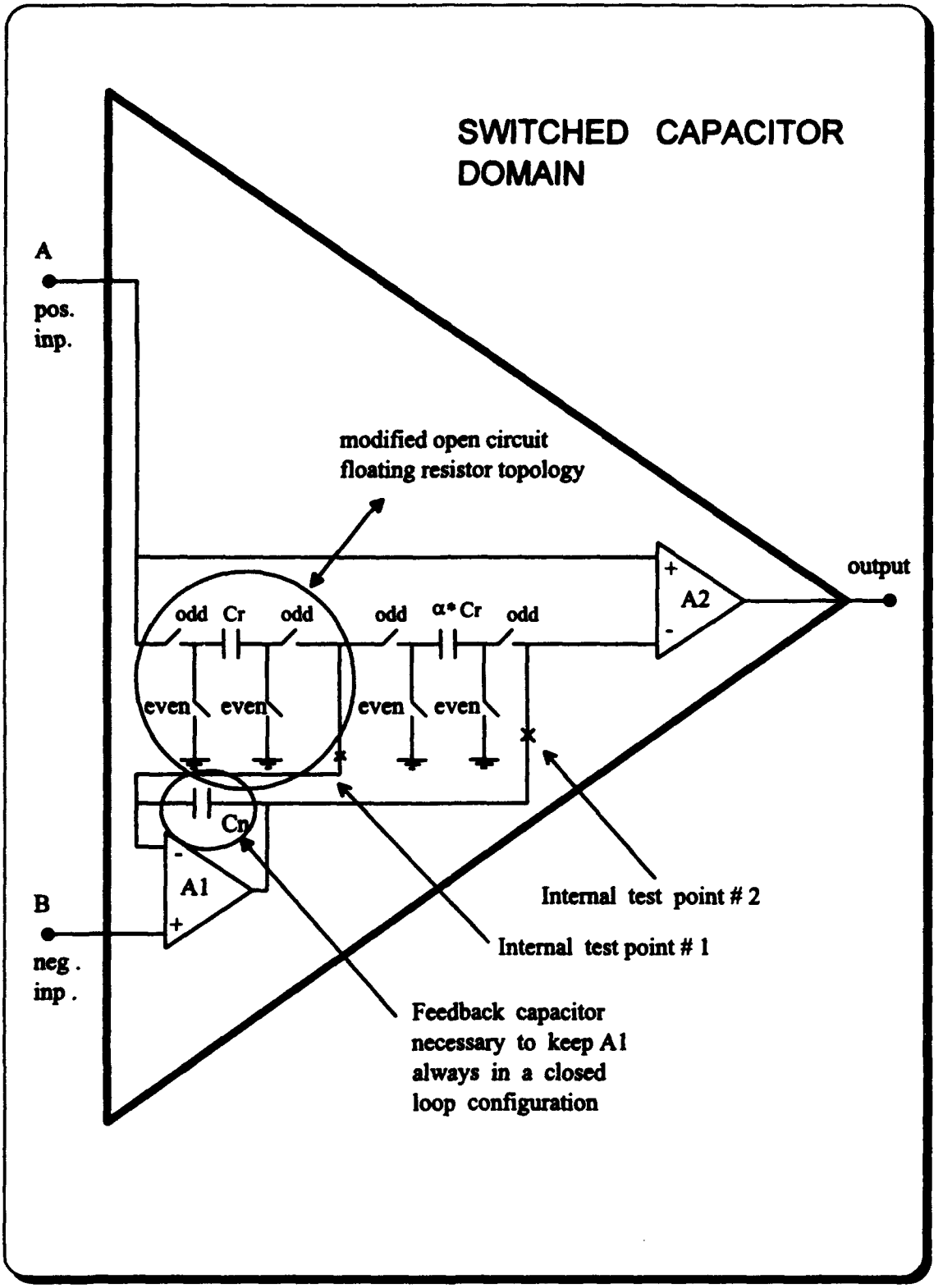


Figure 6.4 Stray Insensitive MOFR C2OA-1

C. Z-DOMAIN EQUIVALENT CIRCUIT MODELS

1. General four port modeling for TSI and MOFR

As mentioned in section A of this chapter, there are some tools to analyze the SC building blocks. Some of these are the multiport equivalent z-domain circuits, which are derived in reference 13. The general equivalent circuits for the TSI and MOFR are listed in Figures 6.5 and 6.6 respectively. They are derived in their most general 2n-port form, assuming that all voltages update at one-half clock cycle intervals. The *"e,o"* notation refers to the switch phasings. Similarly, superscripts *"e,o"* and *"o,e"* are used to denote the even or odd port-variable (V_i , ΔQ_i) components and the complementary odd or even port-variable components, respectively. This *"e,o"* notation conveniently provides the connectivity information for interconnecting the building blocks. The operation of TSI is similar to the MOFR element, with the exception that in TSI the voltage is inverted as the charge on C is transferred from port 1 to port 2. This process is described by the following equations

$$\Delta Q_1^{e,o}(z) = C * V_1^{e,o}(z) + C * z^{\frac{-1}{2}} * V_2^{o,e}(z) \qquad (6.6)$$

$$\Delta Q_1^{o,e}(z) = 0 \qquad (6.7)$$

$$\Delta Q_2^{e,o}(z) = 0 \qquad (6.8)$$

$$\Delta Q_2^{o,e}(z) = C * V_2^{o,e}(z) + C * z^{\frac{-1}{2}} * V_1^{e,o}(z) \qquad (6.9)$$

These equations are readily interpreted by the four-port equivalent circuit in Figure 6.5.

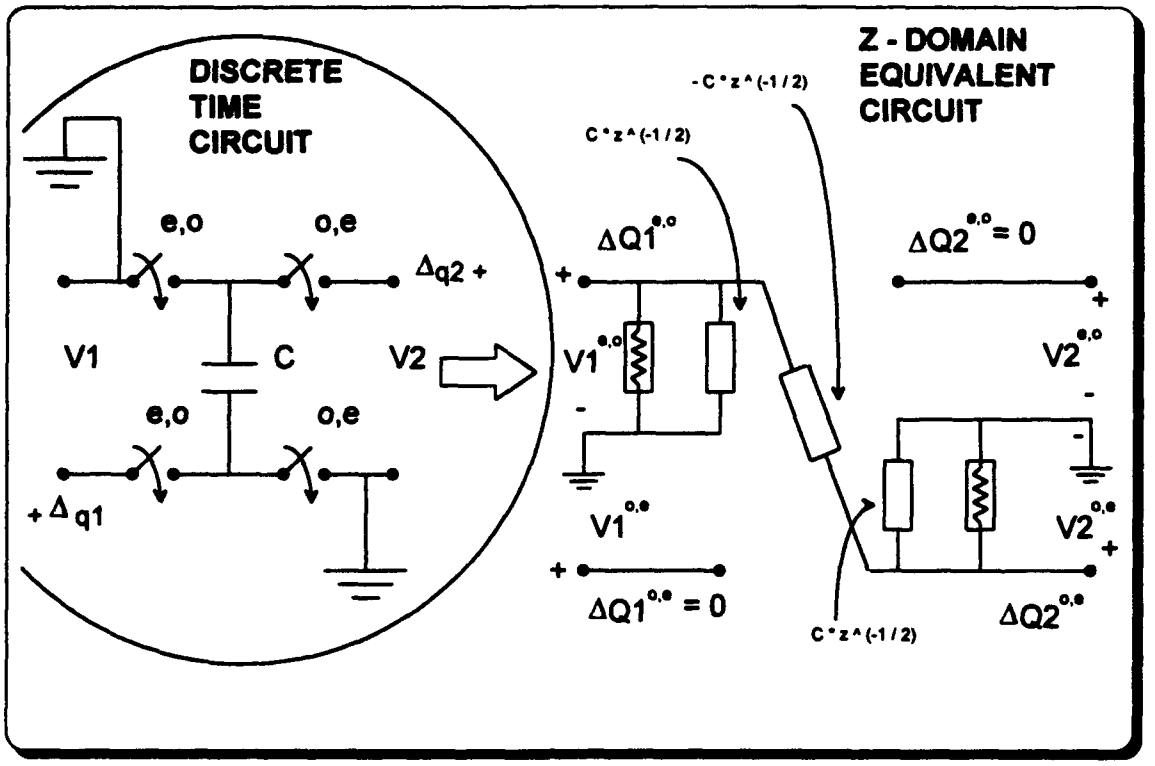


Figure 6.5 General Library Equivalent Model for Toggle Switched Inverter

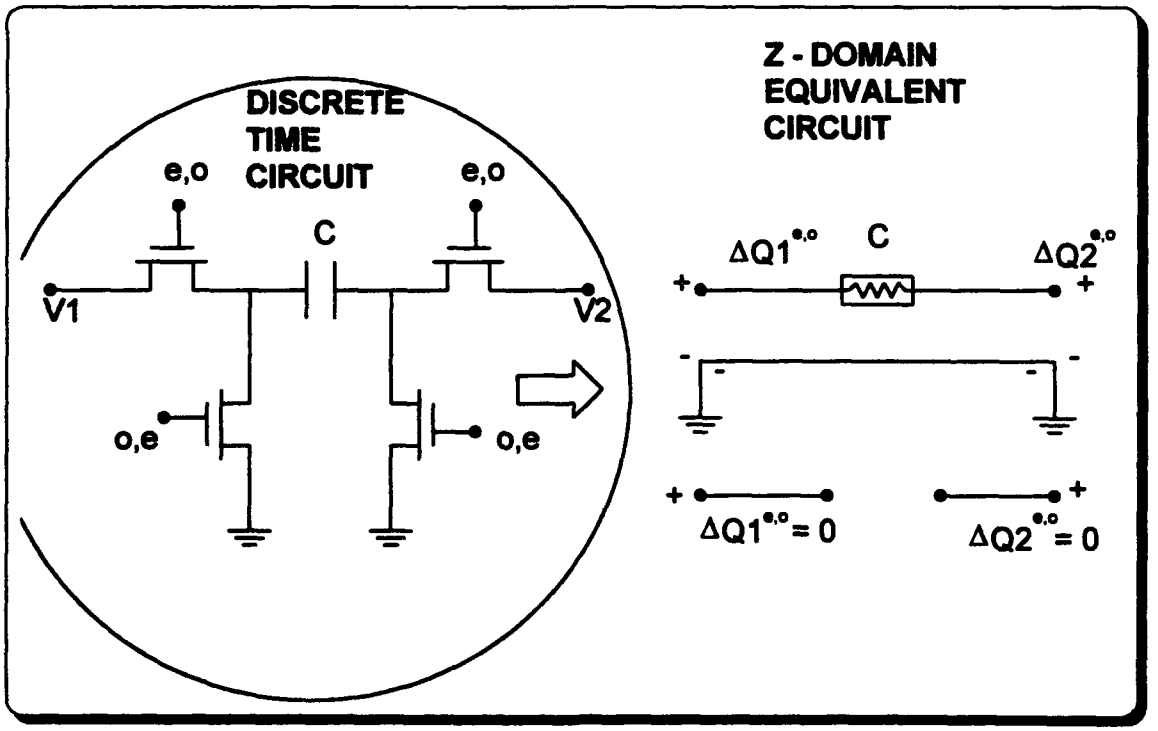


Figure 6.6 General Library Equivalent Model for Modified OFR

2. Full cycle sample and hold assumption

In practice, there are many SC networks in which the charges and voltages update, because of the internal switching action of the SC network only on full clock-cycle intervals. This behavior, which is readily identified on a block-by-block basis, results in 2n-port equivalent circuits with n open ports. When properly interconnected, these 2n-equivalent circuits can be reduced to the n-port equivalent circuits. The equivalent transformation of the individual single amplifiers that are used in the design is first derived. The form of the input signal and the timing of the switches will be taken into consideration. The odd and even phase will always be assumed to be non-overlapping clocks with a 50 % duty cycle. In addition, it is assumed that the input signal is sampled and held over a full clock period, τ=2*T. Thus

$$V_{in}^{o}(z) = z^{\frac{-1}{2}} * V_{in}^{e}(z) \qquad (6.10)$$

The output voltages appearing at the op amp outputs are also held for the full clock period and change only at the even sampling instants

$$V_{out}^{o}(z) = z^{\frac{-1}{2}} * V_{out}^{e}(z) \qquad (6.11)$$

Since both of the input and the outputs are fully held, the even transfer functions provide all the information needed. In Figures 6.7 and 6.8, one can see the simplification in the equivalent circuit of the single amplifier versus the initial 2n-port transformation.

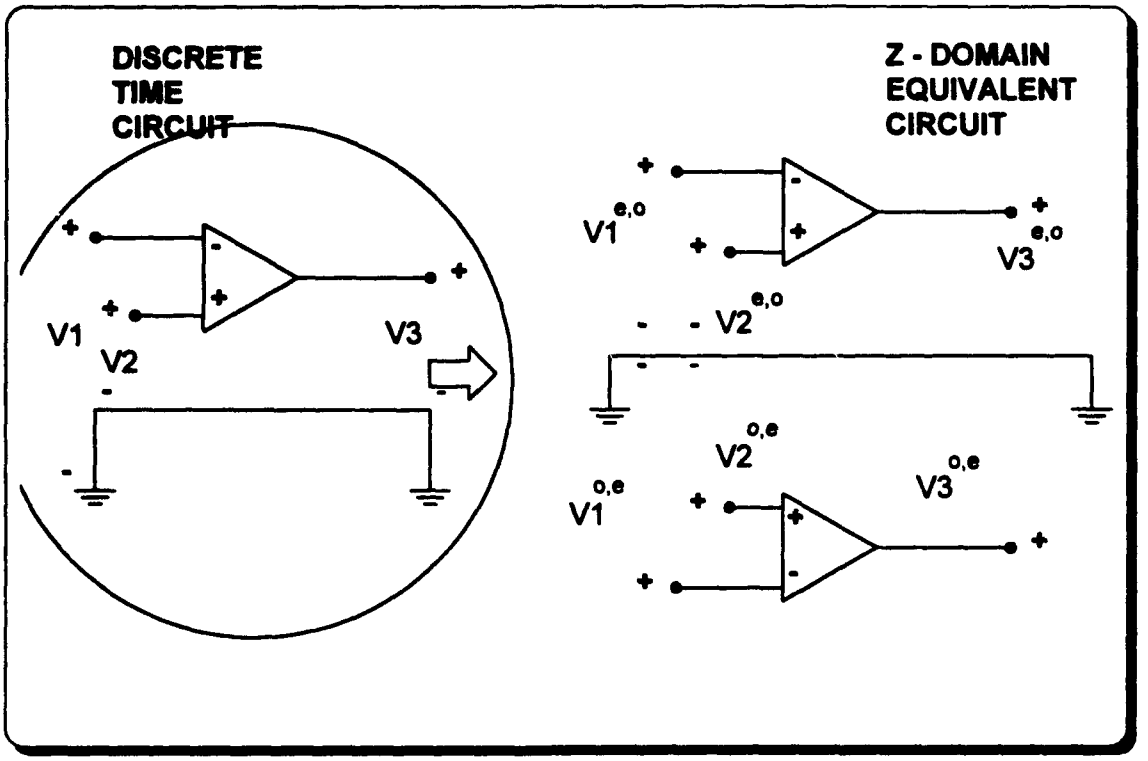


Figure 6.7 General Library Equivalent Single OA

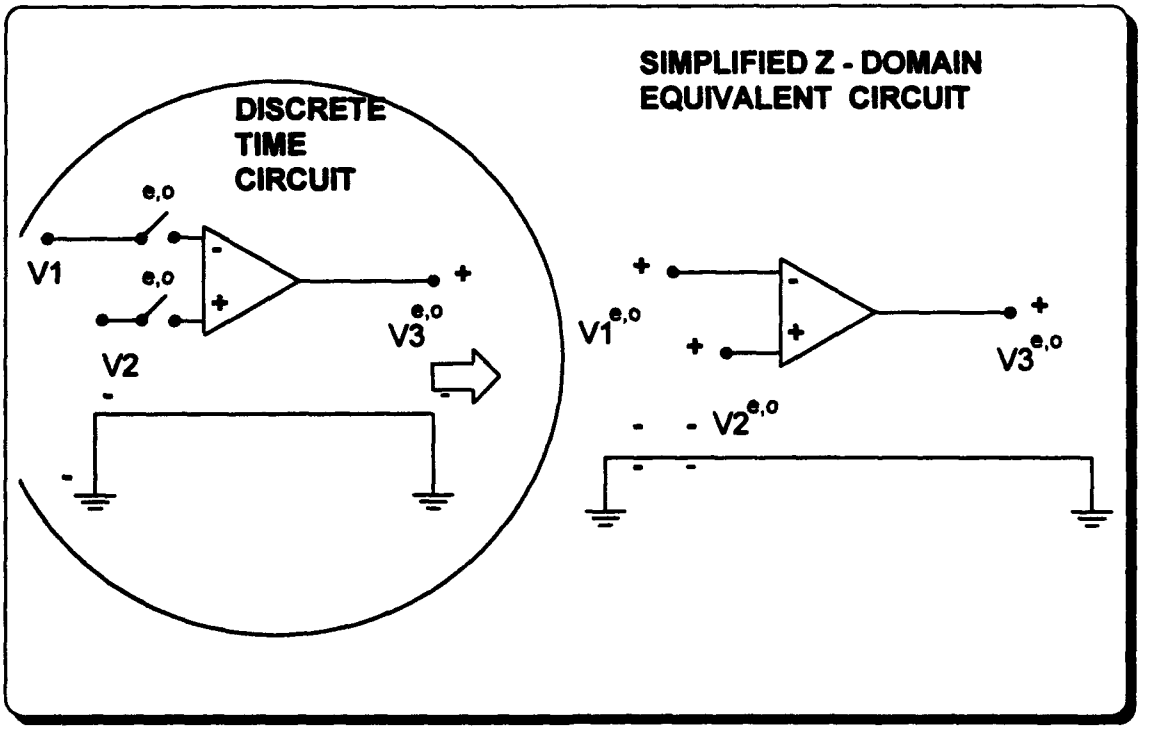


Figure 6.8 Simplified Library Equivalent Single OA

Similarly, Figures 6.9 and 6.10 demonstrate the simplification in the capacitor equivalent when adopting this assumption.

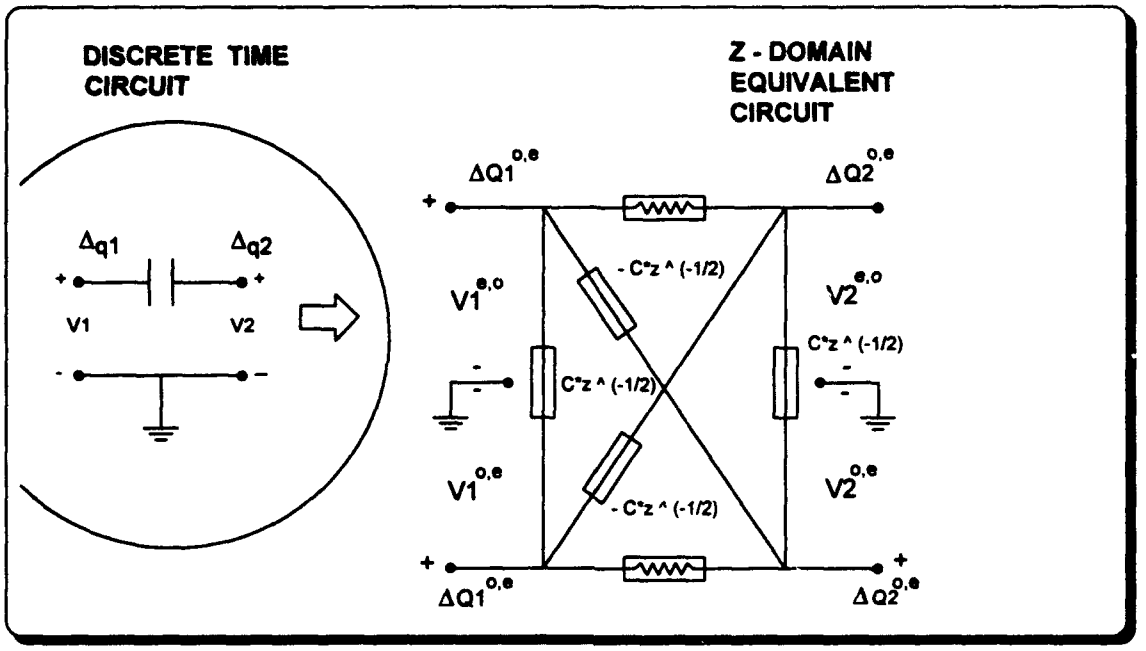


Figure 6.9 General Library Equivalent of Floating Capacitor

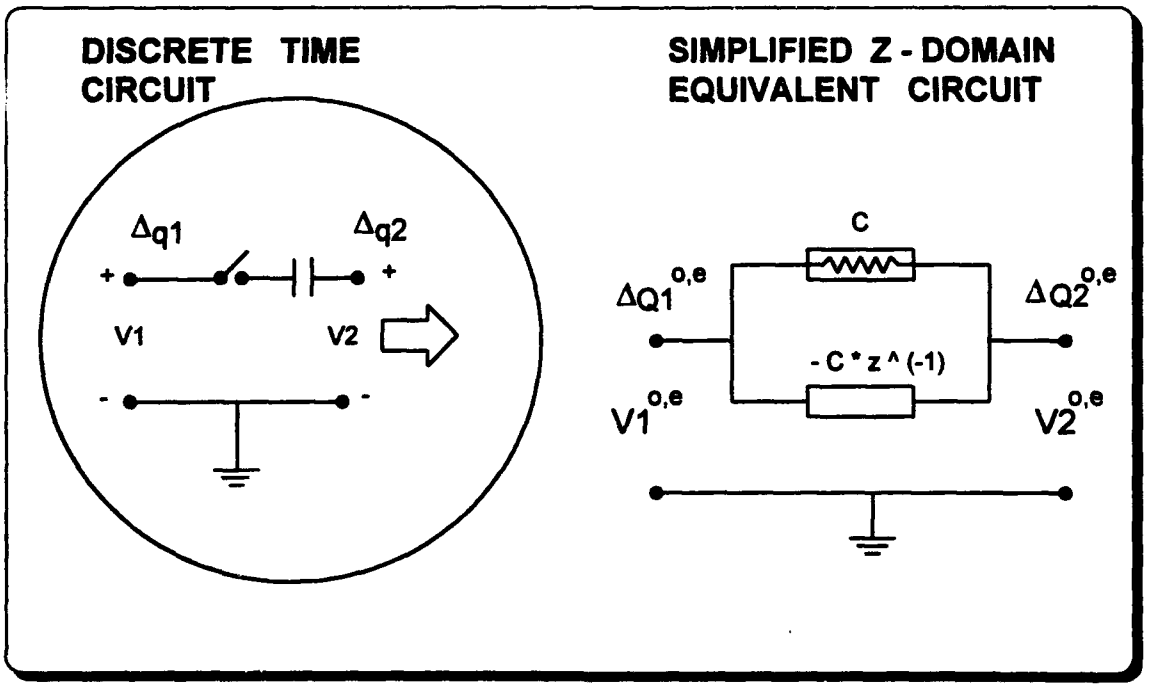


Figure 6.10 Simplified Library Equivalent of Floating Capacitor

3. Mathematical derivation of the z - domain transfer function

a. SC C2OA - 1 : MOFR damping - Open loop transfer function using ideal single operational amplifiers : (Finite gain in infinite bandwidth)

The schematic of the composite C2OA-1, using MOFR damping, and ideal single OAs is shown in Figure 6.11.

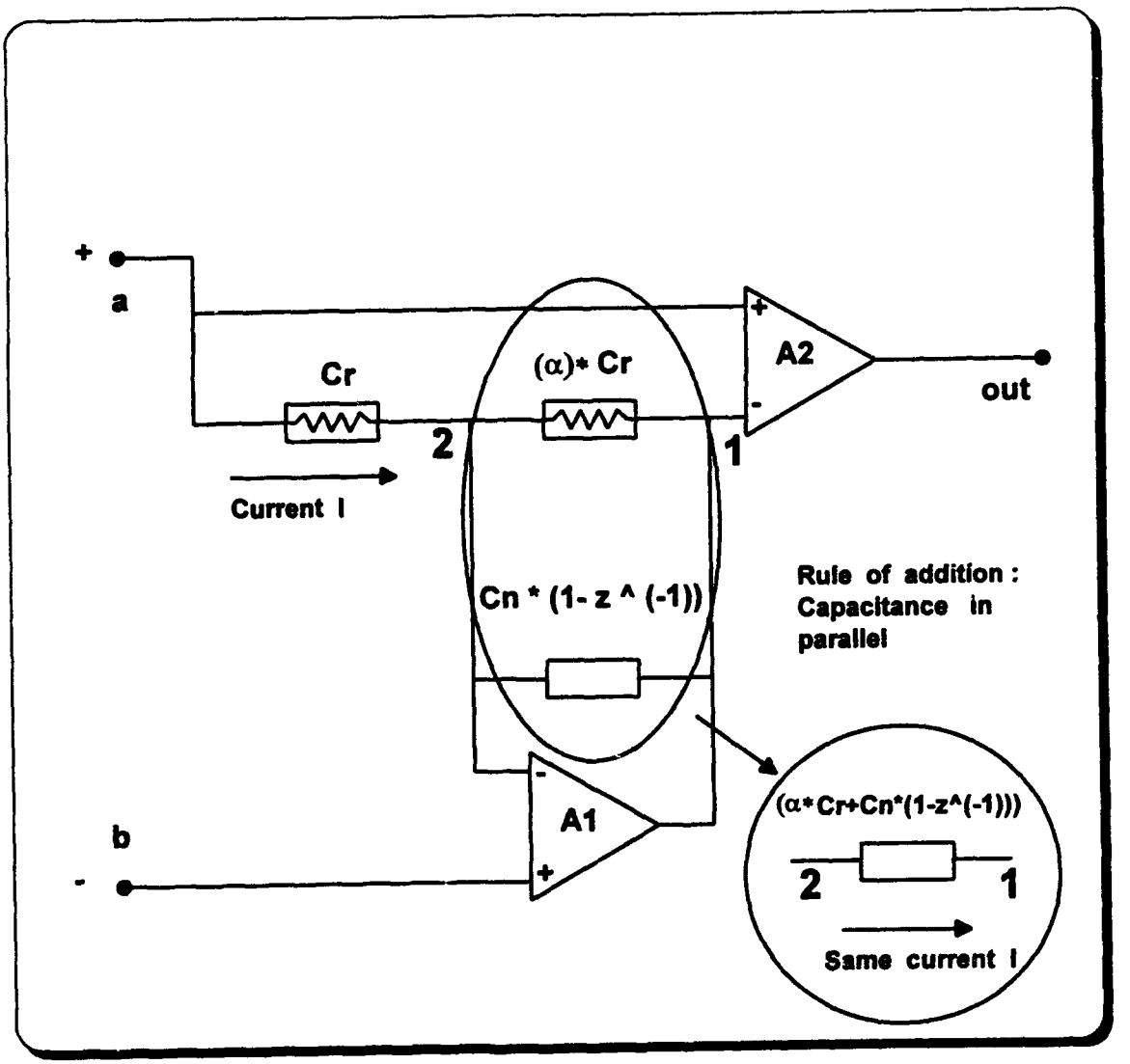


Figure 6.11 C2OA1 - MOFR Equivalent Circuit From the Simplified SC Library

By further simplification of these networks, a new equivalent network would be formed, where simple continuous analysis techniques can be used. Now, applying Kirchoff's laws on that network, the open loop transfer function can be derived. Vout is expressed as a function of Va and Vb, which are the positive and negative inputs respectively. The rule of thumb states that since there are 2 inputs, 1 output, and 2 nodes, we need (2(=number of nodes)+1) equations with unknown variables, the output voltage and the node voltages. The purpose is to get rid of V1 and V2,and then find the relationship Vout = f (Va, Vb). It has been decided to solve the equations using the software *MATHEMATICA by Wolfram Research* in order to minimize the probabilities of a simple human mistake. The full solution is attached as File #1 in the Appendix A.

The open loop transfer function is then

OLTFC2OA1MOFR =

$$\frac{Vb*(A1A2Cn - A1A2Cnz - A1A2Crz - aA1A2Crz) + Va*(-A2Cn - A1A2Cn + A2Cnz + A1A2Cnz + A2Crz + aA2Crz + A1A2Crz + aA1A2Crz}{-Cn - A1Cn + Cnz + A1Cnz + Crz + aCrz + aA1Crz} \quad (6.12)$$

The result is expressed in the form (Va * Aplus - Vb * Aminus) where :

$$Aplus = \frac{(-A2Cn - A1A2Cn + A2Cnz + A1A2Cnz + A2Crz + aA2Crz + A1A2Crz + aA1A2Crz)}{-Cn - A1Cn + Cnz + A1Cnz + Crz + aCrz + aA1Crz} \quad (6.13)$$

$$Aminus = \frac{-(A1A2Cn - A1A2Cnz - A1A2Crz - aA1A2Crz)}{-Cn - A1Cn + Cnz + A1Cnz + Crz + aCrz + aA1Crz} \quad (6.14)$$

b. SC C2OA - 1 : MOFR damping - Open loop transfer function using real single operational amplifiers (Finite gain and finite bandwidth)

As it is seen from the previous section, the ...gle OAs have been considered to have constant gain A1 and A2 respectively over infinite bandwidth. This is not possible though, and the thought of using the single pole model for the single OAs has been adopted. As it is known from reference 19, pages 77 - 78, the Gain A (s) of an internally compensated operational amplifier may be expressed as

$$A(s) = \frac{A_0}{1+\frac{s}{\omega_b}} \tag{6.15}$$

which for physical frequencies, s = j * ω becomes

$$A(s) = \frac{A_0}{1+\frac{j*\omega}{\omega_b}} \tag{6.16}$$

where A_0 denotes the dc gain and ω_b is the 3 - dB frequency (or break frequency). For frequencies $\omega >> \omega_b$ (about ten times and higher) equation (6.16) may be approximated by

$$A(j*\omega) = \frac{A_0*\omega_b}{j*\omega} \tag{6.17}$$

from which it can be seen that the gain | A | reaches unity, (0 dB) at a frequency denoted by ω_t and given by

$$\omega_t = A_0 * \omega_b \tag{6.18}$$

Substituting in equation (6.17) we get

$$A(j*\omega) \cong \frac{\omega_t}{j*\omega} \Rightarrow A(s) = \frac{\omega_t}{s} \tag{6.19}$$

where ω_t is called the unity-gain bandwidth.

After the single pole model transfer function has been clearly defined, we need to be able to convert it to the same domain of analysis, that means *the equivalent z-domain*. This was introduced in details in references 9 and 20, which provide the proper mathematical expression that allows to transform rational s-domain transfer functions to rational z-domain transfer functions. To be generally useful, such an expression must satisfy two conditions

(1) Stable s-domain transfer functions map into stable z-domain transfer functions.

(2) The imaginary $j * \omega$ axis of the s-plane maps onto the unit circle of the unit plane.

Item 1 ensures that the stability information would remain the same, while item 2 ensures that the shape of the gain response would be preserved. One possible transformation expression that satisfies the above conditions is shown below

$$\frac{1}{s} = \frac{\tau}{2} * \frac{1+z^{-1}}{1-z^{-1}} \qquad (6.20)$$

This is called the bilinear transformation and will help to convert equation (6.19) to

$$A(s) = \frac{\omega_t}{s} \Rightarrow A(z) = \omega_t * \frac{\tau}{2} * \frac{1+z^{-1}}{1-z^{-1}} \qquad (6.21)$$

where τ is the sampling interval. The transfer function of the non-ideal composite SC C2OA-1 is found in File # 2, of Appendix A, because of its length, together with the full solution. It is expressed again in the form

Va * Aplus - Vb * Aminus, where Aplus is the positive input contribution and Aminus is the inverting input contribution.

c. SC C2OA - 1 : MOFR damping - Application # 1 : Buffer

We recall from chapter II the Figure 2.4 of the Voltage follower or buffer. The I / O relationship is

$$V_o = V_a * A^+ - V_b * A^- = V_{input} * A^+ - V_{output} * A^- \Rightarrow$$
$$\frac{V_{output}}{V_{input}} = \frac{A^+}{1+A^-} \qquad (6.22)$$

The following component values have been chosen to verify the exactitude of the application

$\omega_{t1} = \omega_{t2} = 6.5285$ MHz
Cr = 1 picoFarad
Cn = 6 picoFarad
Capacitor ratio $\alpha = 1$
Clock = 1 MHz $\Rightarrow$ Sampling interval $\tau = 1$ microsec (6.23)

The symbolic and numeric transfer function of the buffer configuration can be found in Appendix A, File # 3. Now after the transfer function has been derived, it needs to be tested for stability and correctness of results. The stability will be examined through the position of poles with respect to the unit plane (they are shown in Figure 6.12). The correctness of the results will be examined through the transient response, shown in Figure 6.13, and the frequency response, shown in Figure 6.14, of the system. The *MATLAB software version 4.0 with SIMULINK by Mathworks* has been adequate for these tests.

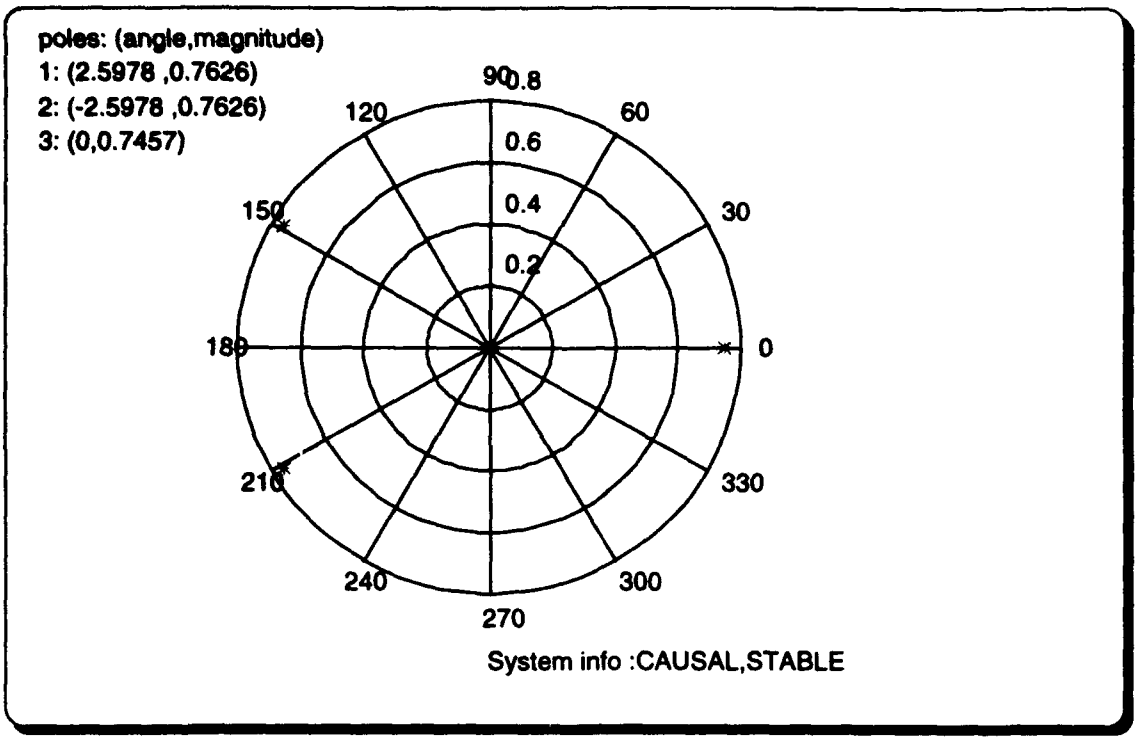


Figure 6.12 C - 20A - 1 Real : MOFR Damping, Buffer, (α) = 1, Pole Plot

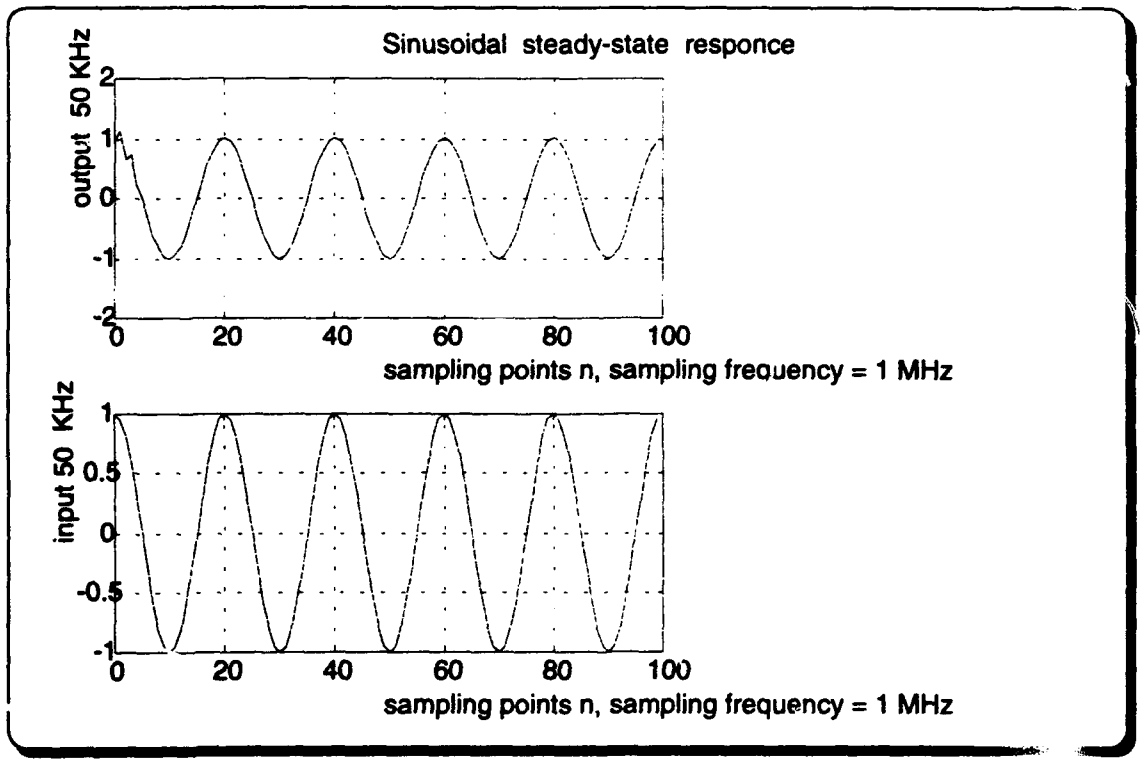


Figure 6.13 C - 20A - 1 Real : MOFR Damping, Buffer, (α)=1, Transient Analysis

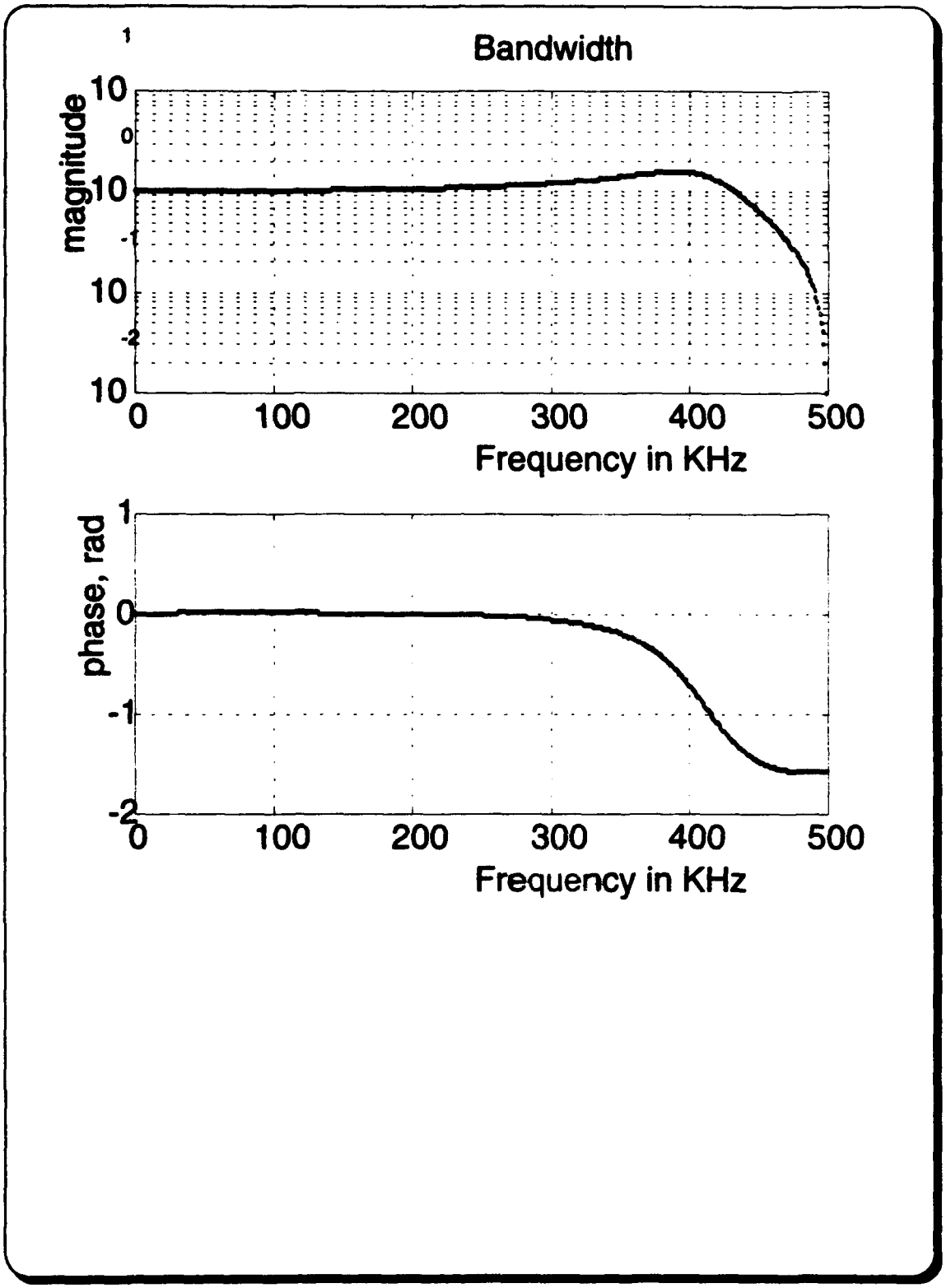


Figure 6.14 C - 20A - 1 Real : MOFR Damping, Buffer Configuration, (α)=1, Sampling Frequency = 1 MHz , Frequency Response

d. SC C2OA - 1 : MOFR damping - Application # 2 : Inverter with gains of -1 and -100.

Recalling from Chapter II, Figure 2.3 of the inverting amplifier configuration, two external resistors R1 and R2 which provide the negative feedback for this amplifier configuration are noticed. The output with respect to the input is given by the equation

$$\frac{V_{output}}{V_{input}} = \frac{(A^- * R2)}{-R1-(A^- * R1)-R2} \qquad (6.24)$$

The derivation of this equation is provided in Appendix A, File # 4. The inverting transfer function for the composite design, after substituting the values for Aminus that were found from the derivation of the real open loop transfer function, is given in Appendix A, File # 5. The following component values have been initially chosen to verify the exactitude of the application

$\omega_{t1} = \omega_{t2} = 6.5285$ MHz
Cr = 1 picoFarad
Cn = 6 picoFarad
Capacitor ratio $\alpha = 1$
Clock = 1 MHz
Sampling interval $\tau = 1$ microsec
R1 = 5 KΩ
R2 = 5 KΩ (6.25)

The stability information is provided in Figure 6.15, the sinusoidal steady-state response is provided in Figure 6.16, and the frequency response is provided in Figure 6.17.

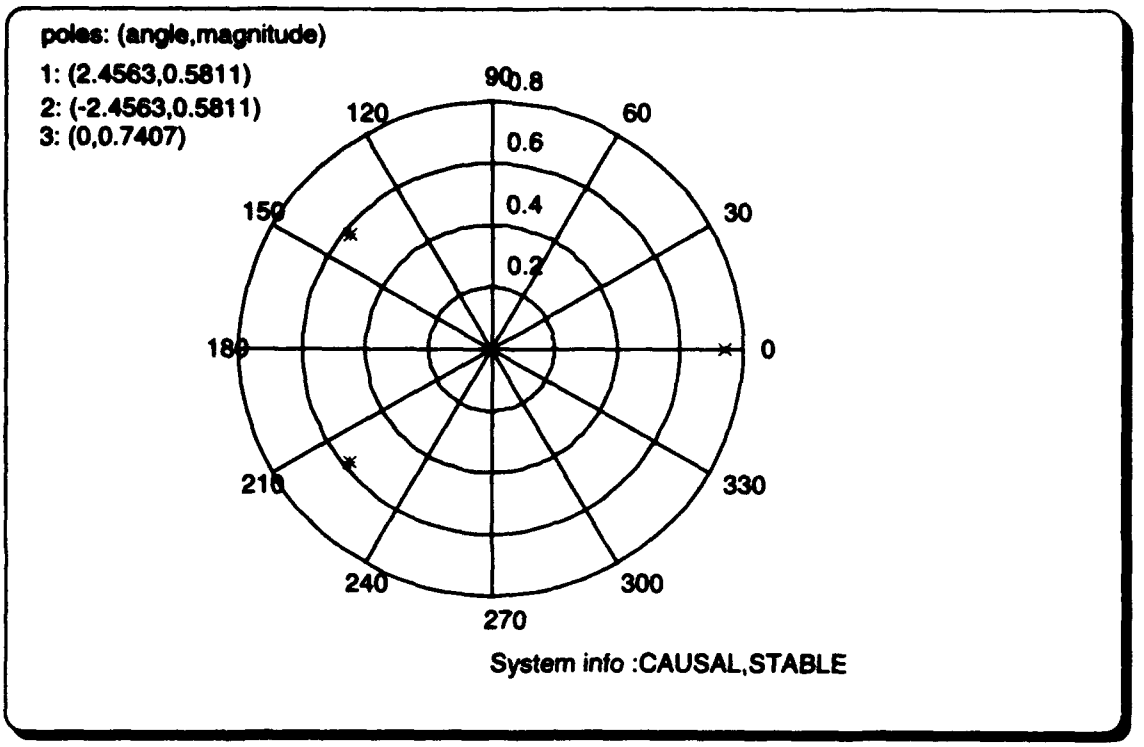


Figure 6.15 C - 2OA - 1 Real : MOFR Damping, Inverter, (α)=1, Gain = -1, Pole Plot

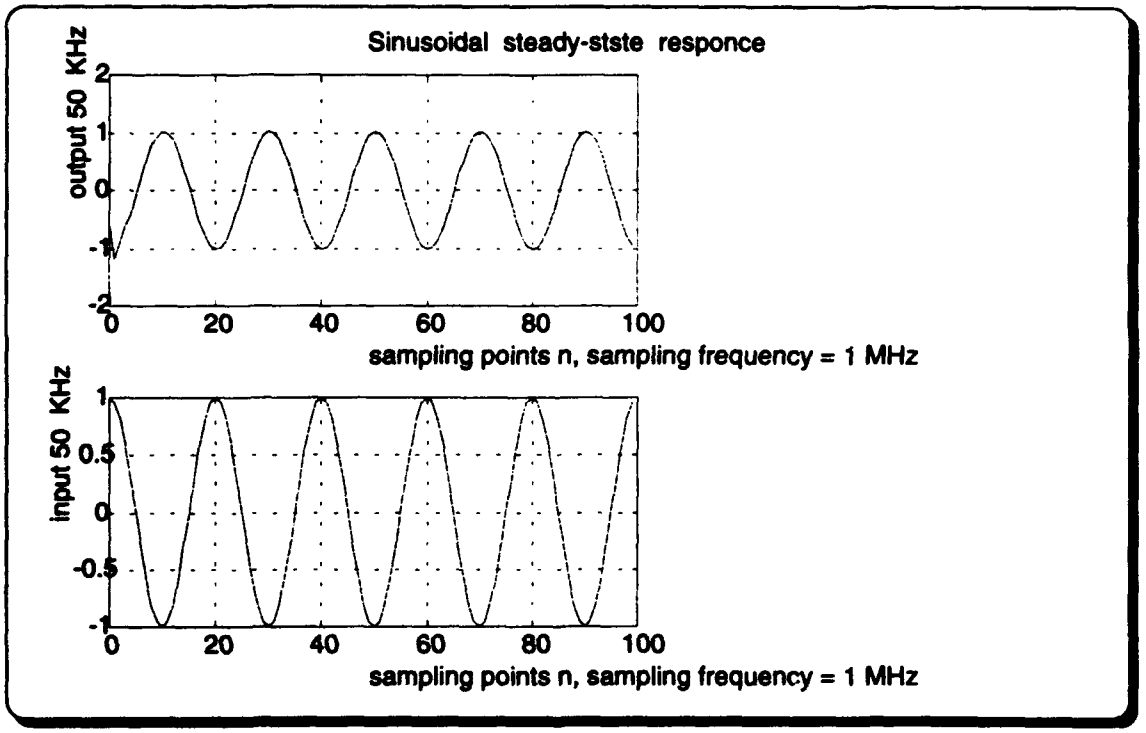


Figure 6.16 C - 2OA - 1 Real : MOFR Damping, Inverter, (α)=1, Transient Analysis

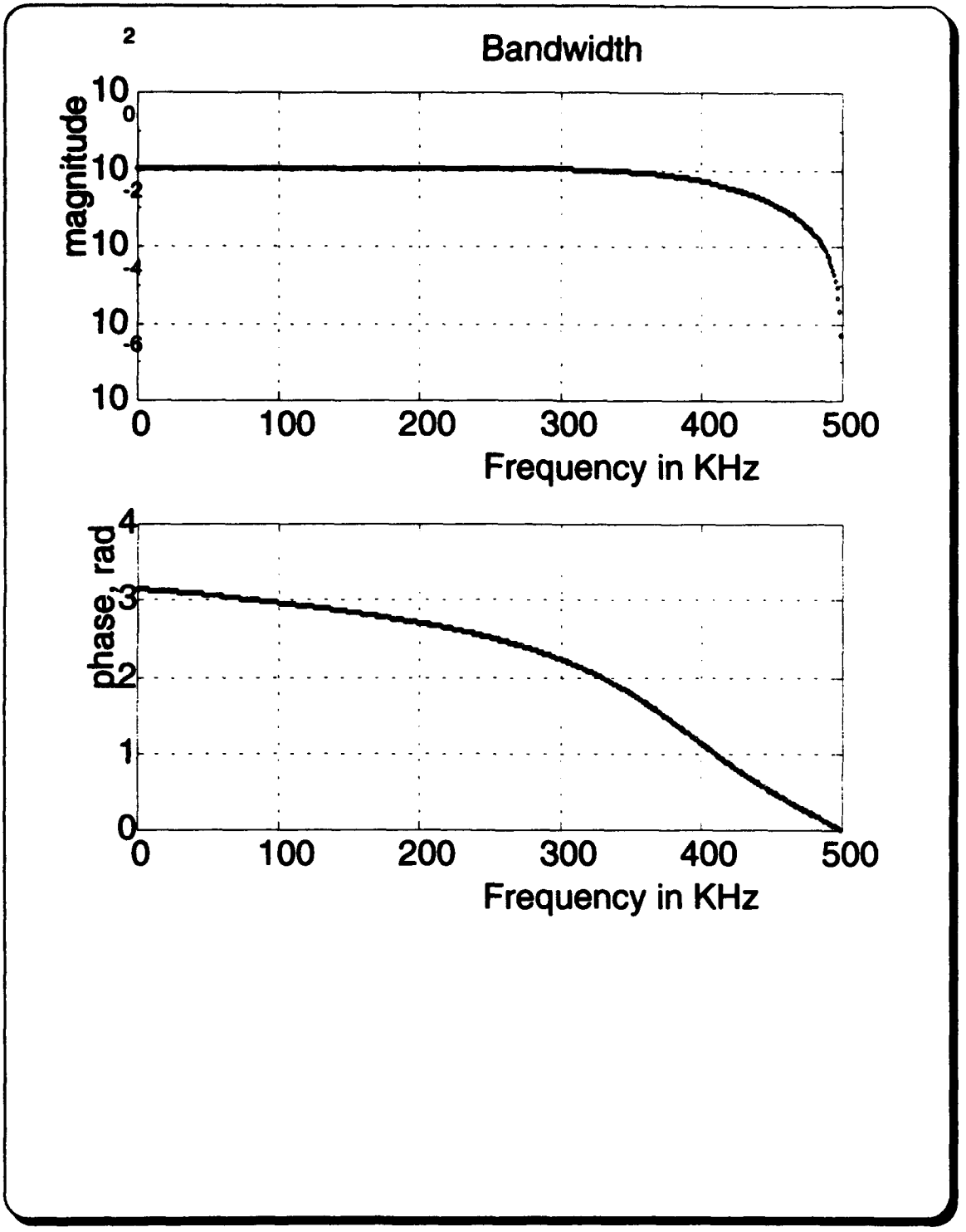
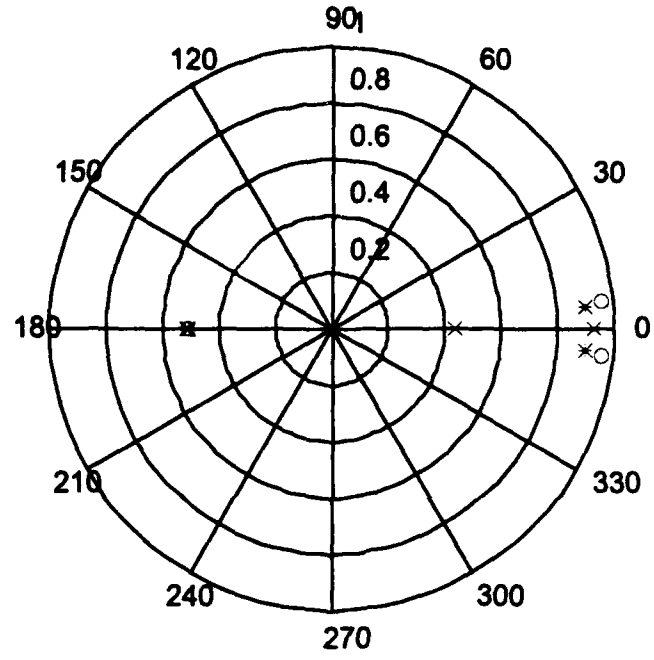


Figure 6.17 C - 2OA - 1 Real : MOFR Damping, Inverting Configuration, (α)=1, Sampling Frequency = 1 MHz , Gain = -1, Frequency Response

All the components of the first test remained the same except the values of R2 and R1 which became 50 KΩ and 500 Ω respectively, created a negative feedback ratio of -100 and the values of α which varied from 0.1 to 8. Solutions for the new transfer functions are then given in Appendix A, Files #6, #7 and #8. The position of the poles in all three cases is shown in Figure 6.18 for comparison reasons. The sinusoidal response for all cases is shown again in Figure 6.19 and the frequency response in Figure 6.20.



Poles information	
Capacitor ratio (α) 0.1	
Magnitude	Angle (rad)
0.9592	0.0992
0.9592	- 0.0992
0.5071	3.1416

Poles information	
Capacitor ratio (α) = 1	
Magnitude	Angle (rad)
0.8969	0.0886
0.8969	- 0.0886
0.508	3.1416

Poles information	
Capacitor ratio (α) = 8	
Magnitude	Angle (rad)
0.9285	0
0.4365	0
0.5131	3.1416

Figure 6.18 Inverting Configuration for SC C2OA - 1 : MOFR Damping, Gain = -100,

Index : 'o' for (α) = 0.1, '*' for (α) = 1, 'x' for (α) = 8

Poles Position

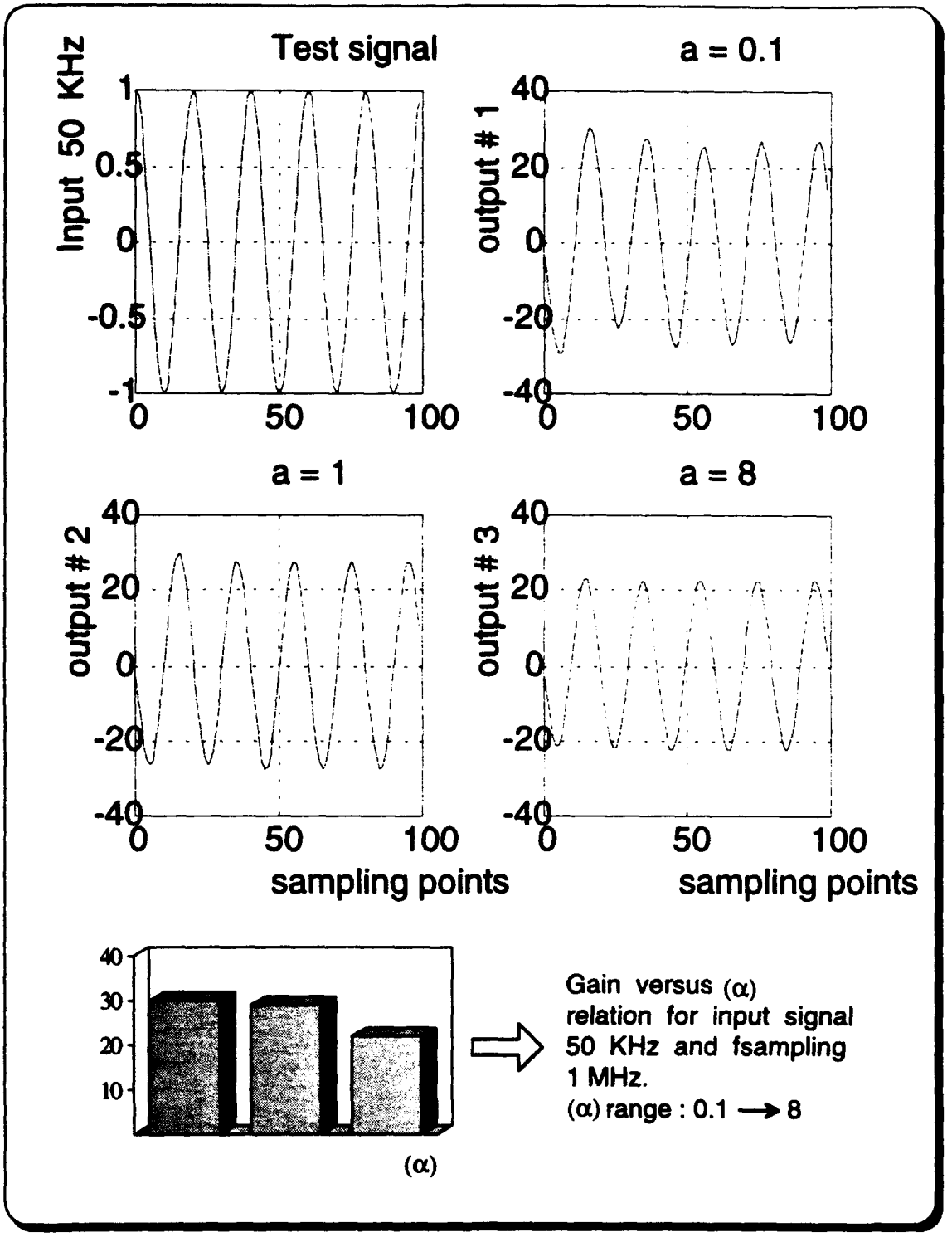


Figure 6.19 Inverting Configuration For SC C2OA - 1 : MOFR Damping, Gain = -100, Sinusoidal Steady-State Response

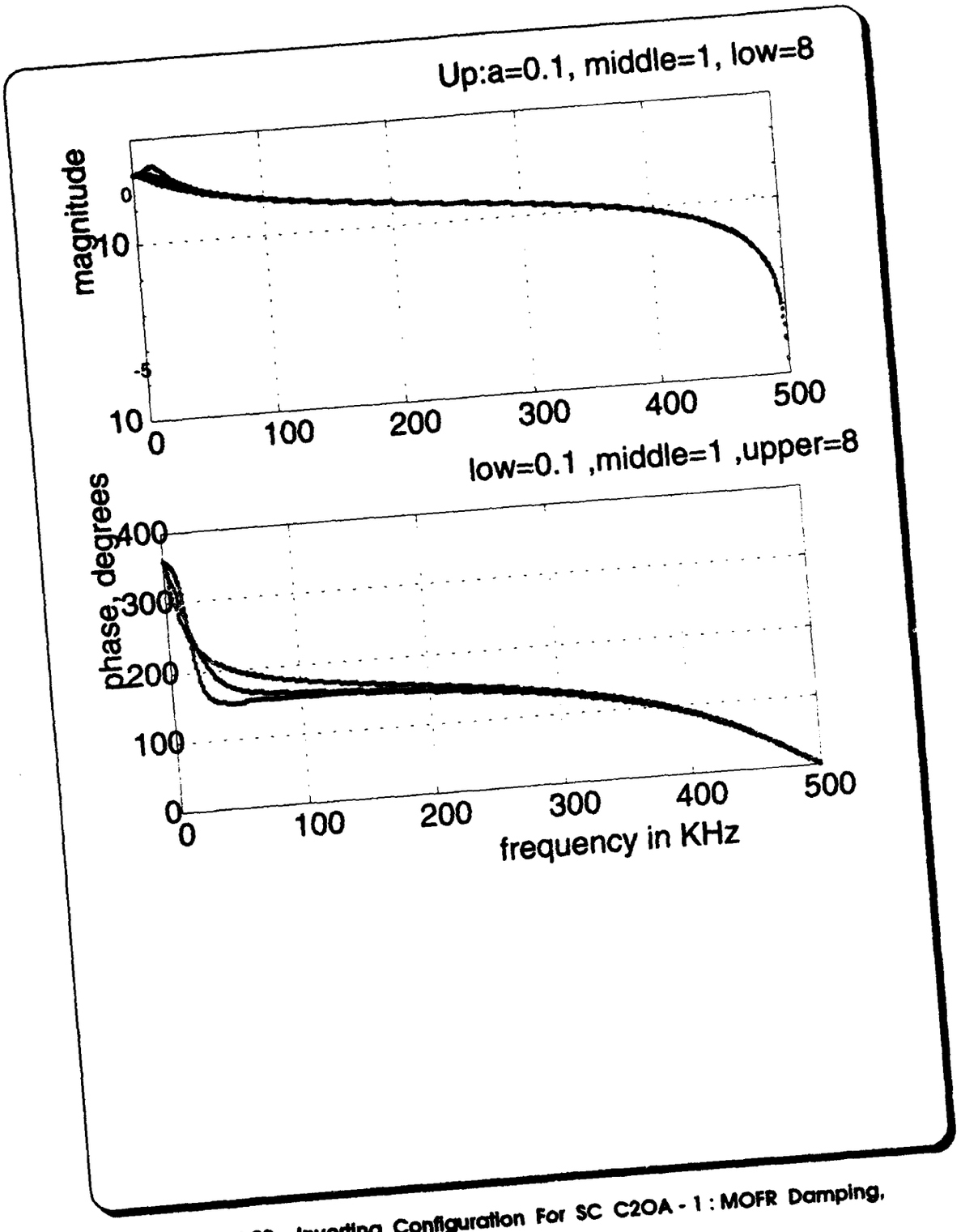


Figure 6.20 Inverting Configuration For SC C2OA - 1 : MOFR Damping, External Resistor Ratio = -100, Frequency Response Plots, Fsamp = 1 MHz

e. SC C2OA - 1 : TSI damping

In this case, the equivalent circuit of the composite amplifier is different due to the difference between the z-domain equivalence of the TSI and the MOFR. The "new" composite is shown then in Figure 6.21.

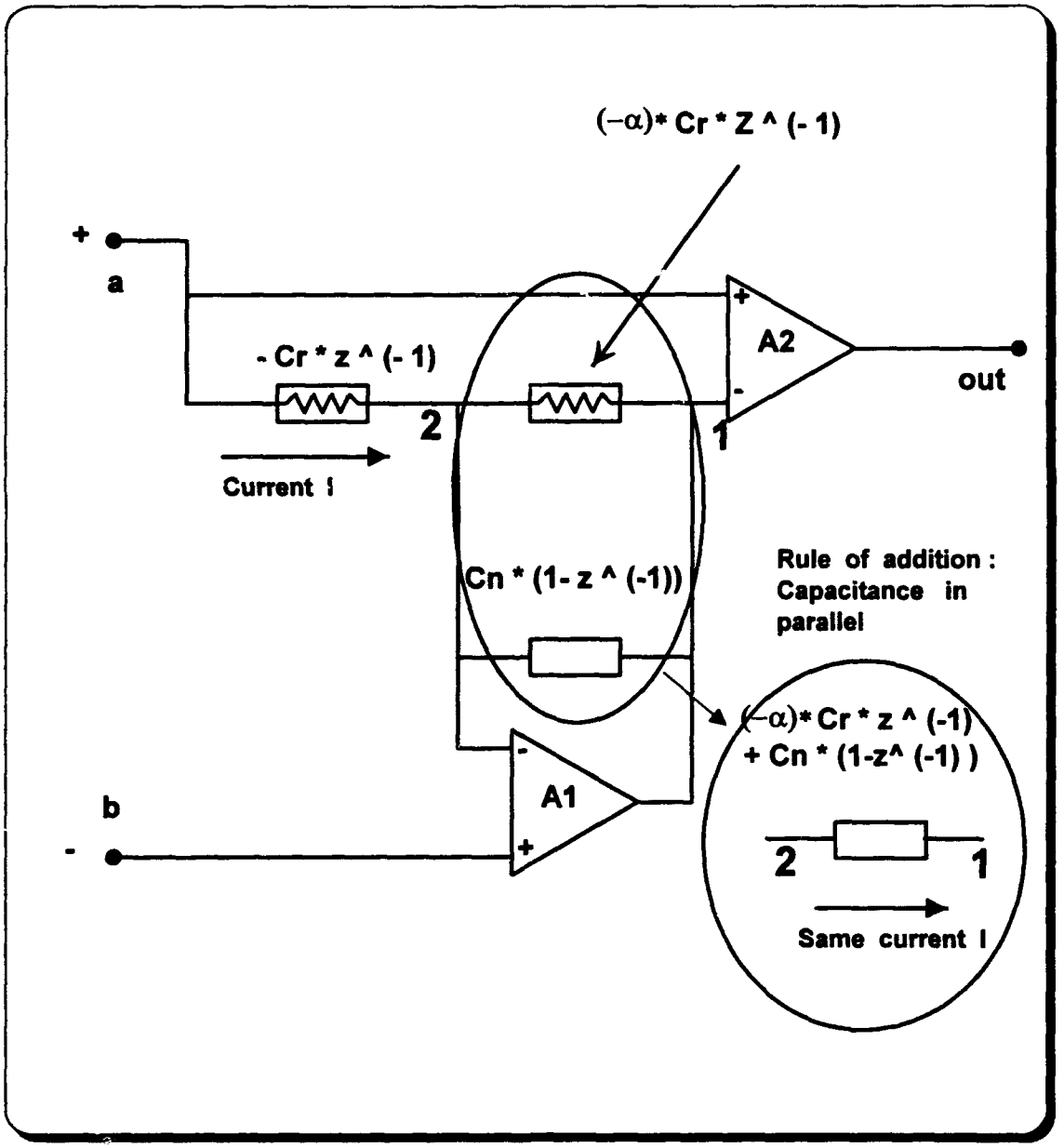


Figure 6.21 Equivalent Circuit Diagram for SC C2OA - 1 : TSI Damping

The full solution of that real circuit is given in Appendix A, File # 9. The transfer functions of the ideal and real open loop case are also derived and expressed in the form Va * Aplus - Vb * Aminus. Finally, the behavior of the circuit in a buffer configuration is examined using the following numerical values

$$\omega_{t1} = \omega_{t2} = 6.5285 \text{ MHz}$$
Cr = 1 picoFarad
Cn = 6 picoFarad
Capacitor ratio $\alpha = 1$
Clock = 1 MHz
Sampling interval $\tau = 1$ microsec (6.26)

The position of the poles is shown in Figure 6.22. The sinusoidal steady-state response for an input sinusoid is given in Figure 6.23. After the first of these two figures the system becomes unstable (since one pole is outside the unit circle). A second simulation is then performed with the value of Cr changed to 0.05 picofarads. The results are shown in Figures 6.24, 6.25 and 6.26. The solution of the transfer function is given in Appendix A, File 10. The system becomes marginally stable and we can get the expected buffer output. The comments for that inconvenience will be included in the conclusions subsection.

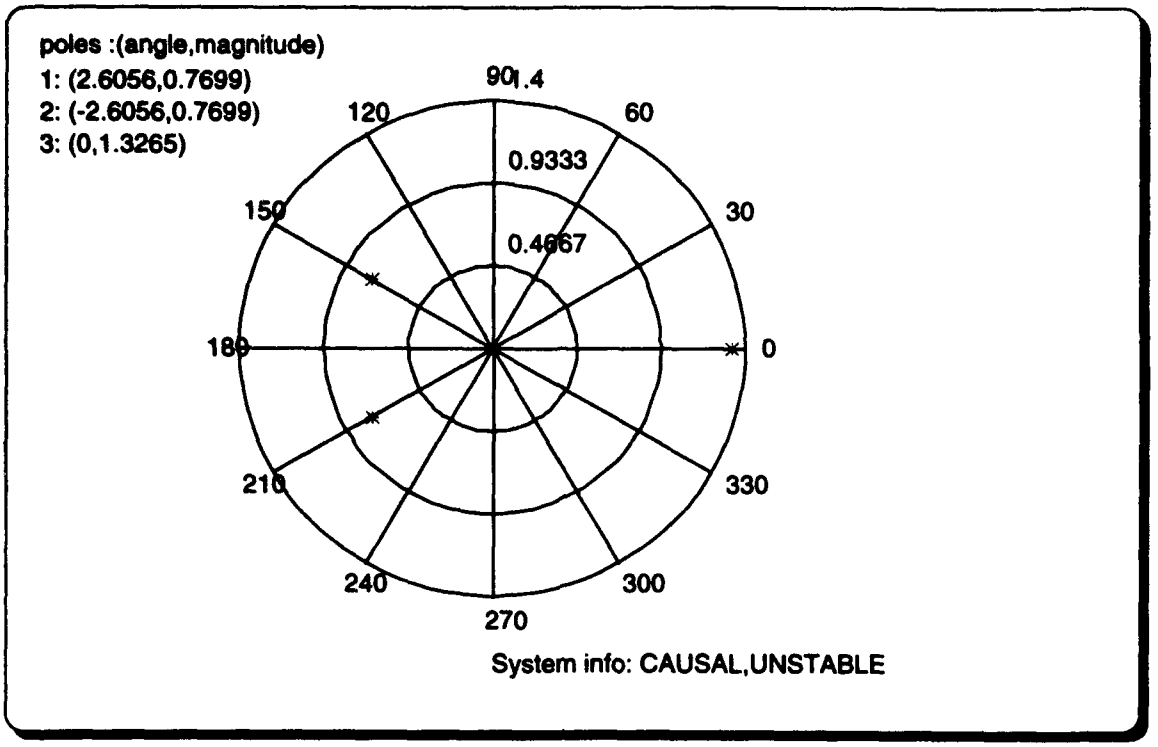


Figure 6.22 C - 20A - 1 Real : TSI Damping, Buffer, Cr = 1 Pico, (α)= 1, Pole Plot

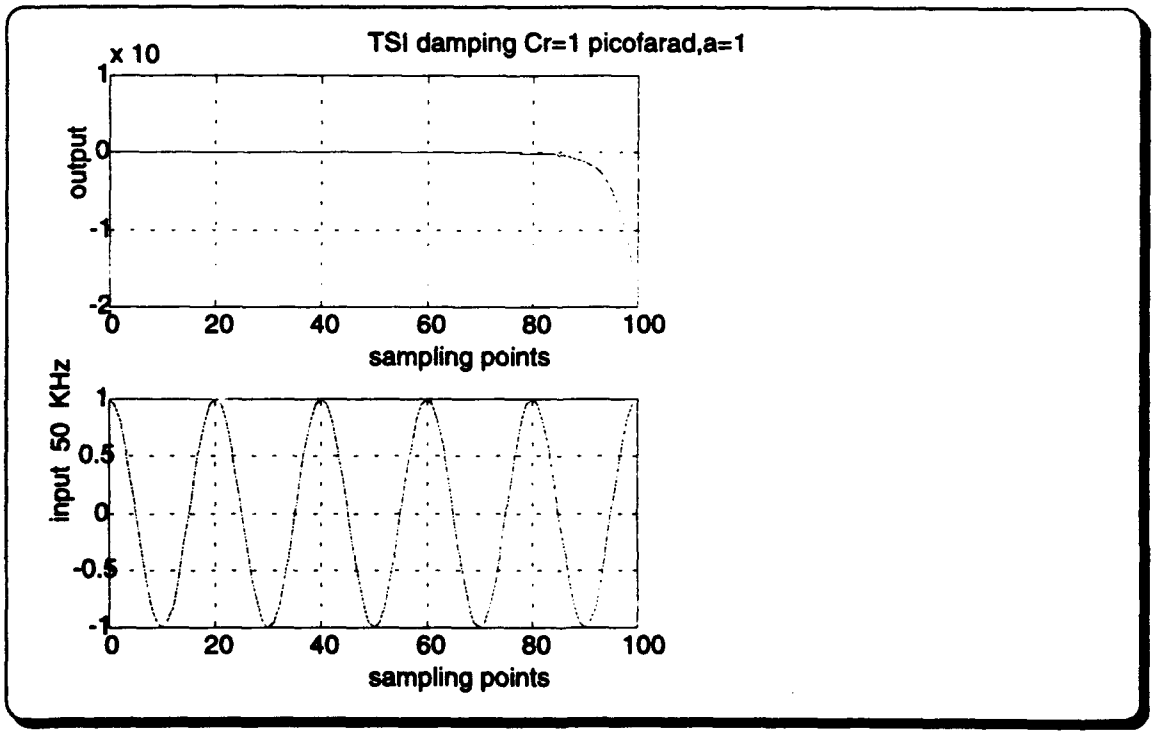


Figure 6.23 C - 20A - 1 Real : TSI Damping, Sinusoidal Steady-State Response

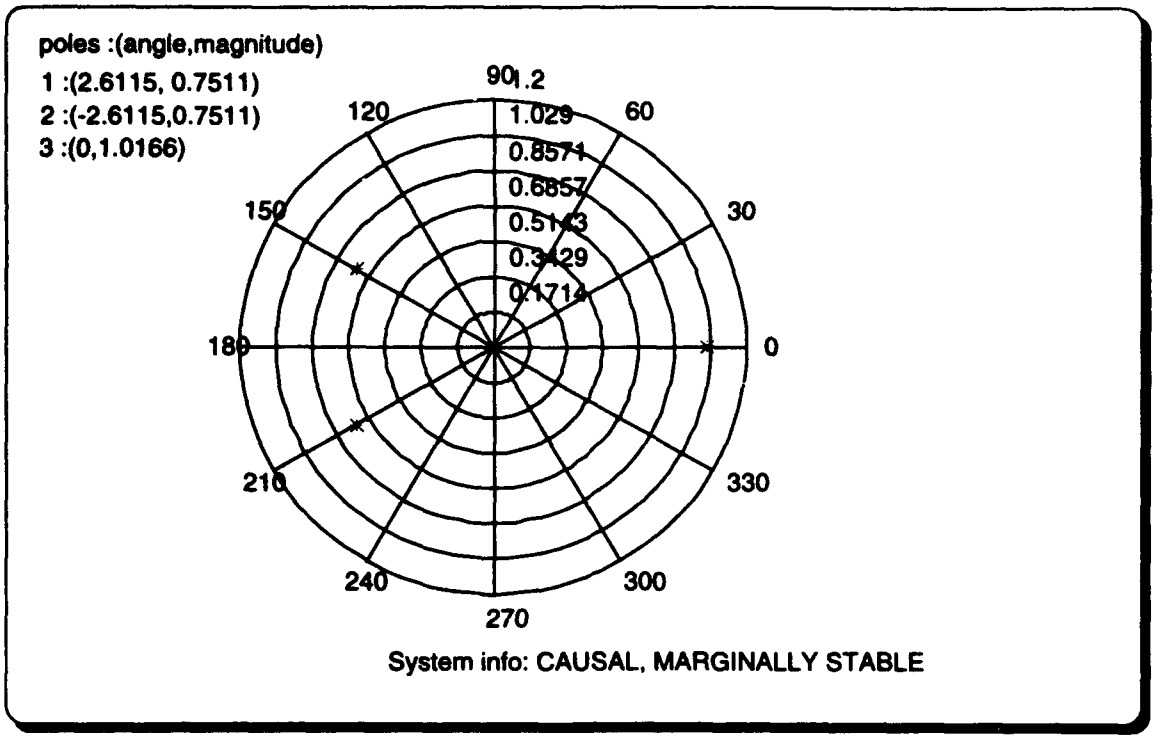


Figure 6.24 C - 2OA - 1 Real : TSI Damping, Buffer, Cr = 0.05 Pico, (α)=1, Pole Plot

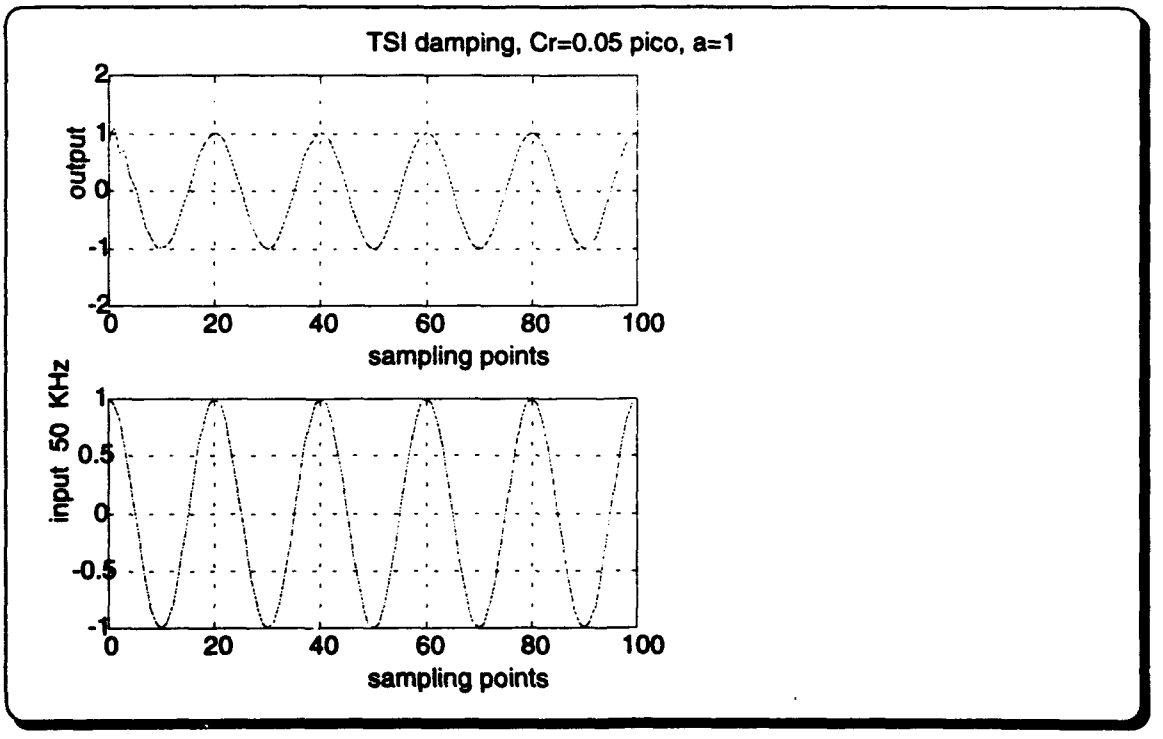


Figure 6.25 C - 2OA - 1 TSI Real : Sinusoidal Steady-State Response, Cr = 0.05 Pico

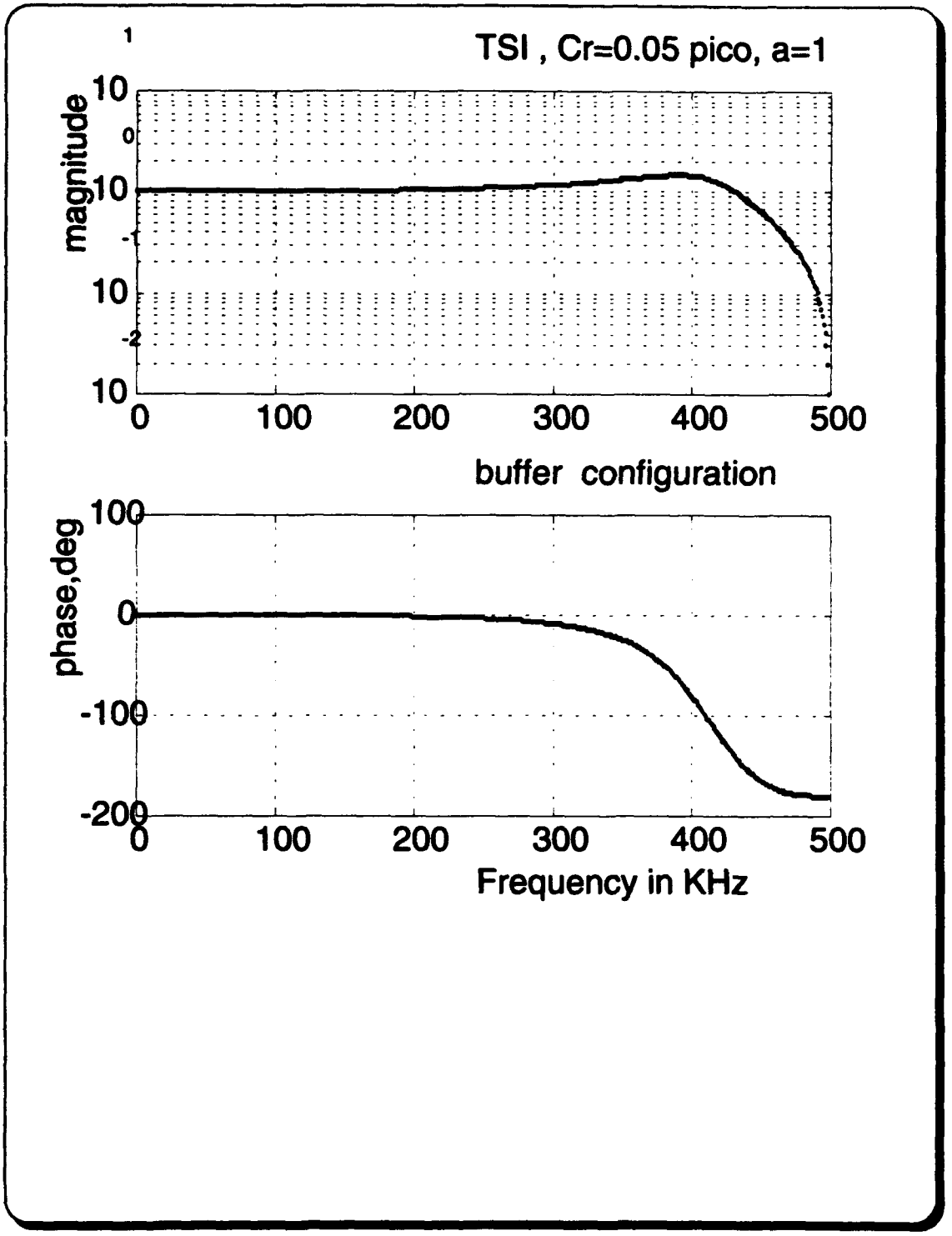


Figure 6.26 C - 2OA - 1 Real : TSI Damping, Sampling Frequency = 1 MHz

Frequency Response

f. Conclusions

It has been shown that one can indeed use the tools of mathematical analysis within the concepts of electric circuits in order to design, verify, or debug switched capacitor amplifier circuits. Therefore, one can compare and verify simulation analysis outputs such as Spice, and predict with more accuracy the expected results of a switched capacitor network, and continue on to the actual implementation of the microchip.

Moreover, it has been proven that the replacement of the resistors in the analog domain by the switched capacitors in the discrete SC domain changes, and sometimes completely reverses, the properties of a circuit first observed as an analog circuit. Of course, both of them are correct, simply for the reason that in reality we have different circuits. As an example for the last statement, let us compare the results of reference 2, page 452, with this investigation. For the C2OA-1, it had been found that, as the ratio α increased, the dc gain increased too. On the other hand, in the switched capacitor domain, Figures 6.18 and 6.19 verify this statement, even though the ratio α increased as the dc gain decreased. The stability of the circuit increased because the poles were moved toward the interior of the unit circle. The results are not contradictory, since the ratio α may be the same variable, but in reality it is the reciprocal of the ratio in the continuous domain. Since R=1 / (Frequency times the Capacitance), it is correct that the conclusions will be of reciprocal meaning.

Furthermore, only now can we verify why the use of the MOFR damping will result in a stable network, while the TSI damping will create problems (as they were faced indeed in reference 14, and were recommended for future research). The reason is that the toggle switched inverter, as indicated from its name, inverts the transfer function, contrary to the MOFR design. Thus, in a specific application, whenever the composite amplifier C - 2OA - 1 is used, it may be a stray insensitive design but it creates positive feedback that decreases the stability of the system. This is why the system requires such a small value of capacitance Cr, which of course works theoretically, but practically it is not a desirable solution. Now that all the preliminary questions are answered, this investigation can proceed to the next chapter where the theory will be converted into an implementation.

VII. VLSI IMPLEMENTATION

A. SILICON SEMICONDUCTOR TECHNOLOGY : AN OVERVIEW

Silicon, in its pure or intrinsic state, is a semiconductor having a bulk electrical resistance somewhere between that of a conductor and an insulator. The conductivity of silicon can be varied over several orders of magnitude by introducing impurity atoms into the silicon crystal lattice. These dopants may either supply free electrons or holes. Silicon that contains a majority of donors is known as n-type and that which contains a majority of acceptors is known as p-type. When n-type and p-type materials are brought together, the region where the silicon changes from n-type to p-type is called a *junction*. By arranging junctions in certain physical structures, and combining these with other physical structures, various semiconductor devices may be constructed.

The basic raw material used in modern semiconductor plants is a *wafer or disk of silicon, which varies from 75 mm to 230 mm in diameter and* is less than 1 mm thick. Wafers are cut from ingots of single crystal silicon that have been pulled from a crucible melt of pure molten polycrystalline silicon. Controlled amounts of impurities are added to the melt to provide the crystal with the required electrical properties. The wafer that has been cut will provide either a p-type or n-type substrate on which the transistors will be produced [Ref. 11 : pp 109 - 117].

B. THE CMOS PROCESS : EPITAXY, DEPOSITION, DIFFUSION AND ION-IMPLANTATION

To build various semiconductor devices, silicon containing varying proportions of donor or acceptor impurities is required. This may be achieved using epitaxy, deposition, or implantation. *Epitaxy* involves growing a single-crystal film on the silicon surface by subjecting the silicon wafer to elevated temperature and a source of dopant material. *Deposition* might involve evaporating dopant material onto the silicon surface followed by a thermal cycle, which is used to drive the impurities from the surface of the silicon into the bulk. What type of impurities are introduced is controlled by the dopant source. How much is used is determined by the energy and time of the *ion-implantation* or the type and temperature of the deposition and diffusion step. Where it is used is determined by using special materials as masks. The ability of these materials to act as a barrier against doping impurities is a vital factor in this process, called *selective diffusion* [Ref. 11. pp : 109 - 124]

The objective of the CMOS process is to provide the capability for NMOS and PMOS transistors on the same substrate. This is realized through wells. The well is an area in the substrate that is created by doping that area with a dopant that is opposite to the type used in the substrate. Thus, a p-well process is one in which the wafer or substrate

is n-type and a well of p-type is added. In an n-well process, the substrate is p-type and a well of n-type is added. Both of these processes allow for the manufacture of both PMOS and NMOS transistors in the same wafer. In Figure 7.1, one can see how a NMOS and a PMOS transistor look like, when fabricated and combined in a N-well process.

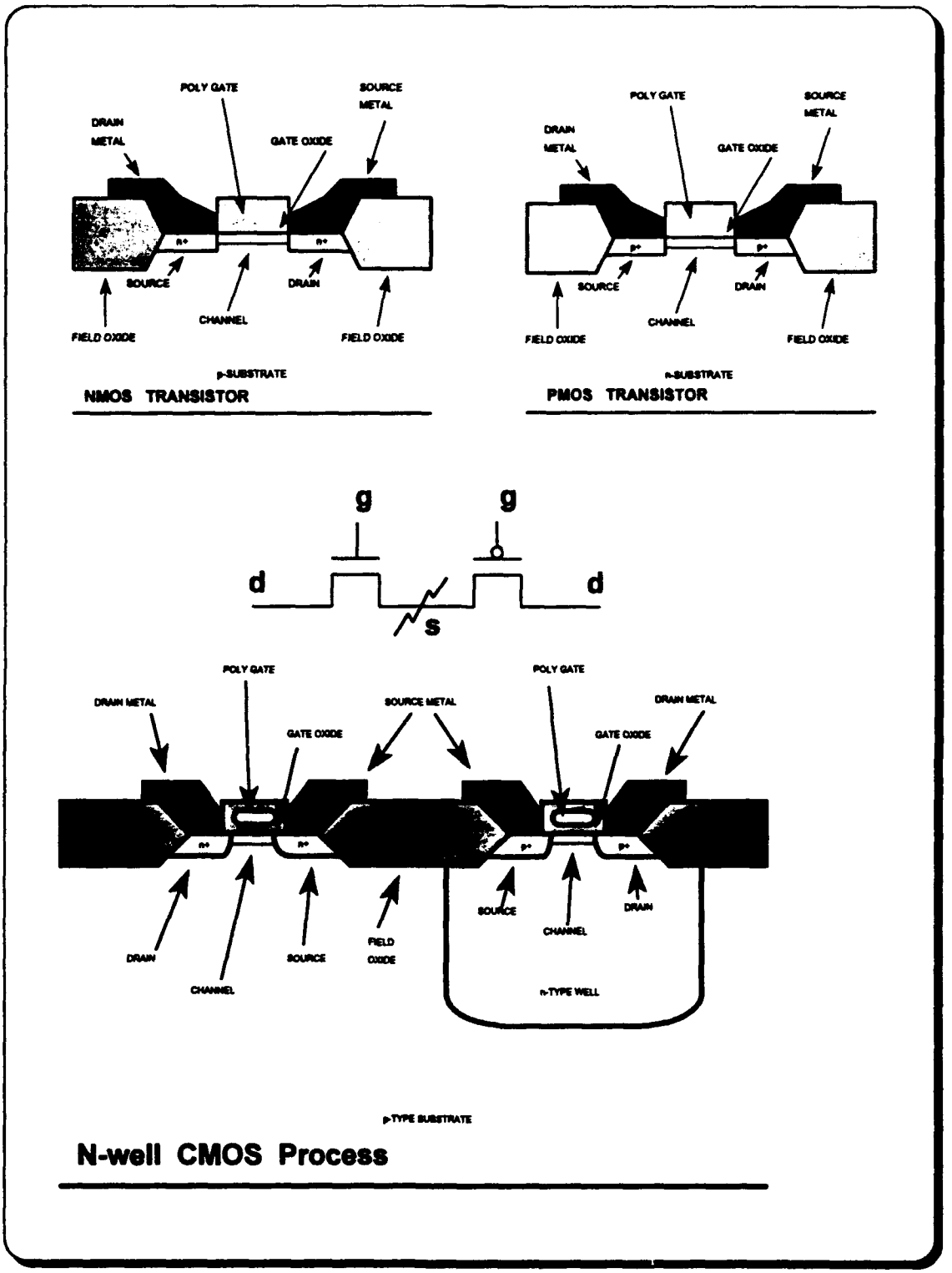


Figure 7.1 Implementation of CMOS Transistor Logic Through the N-Well Fabrication Process.

C. ANALOG INTEGRATED CIRCUITS: DESIGN CONCEPTS AND DIFFICULTIES.

The field of analog integrated circuits is constantly developing and maturing. The initial groundwork was laid in bipolar technology, followed by a rapid evolution of MOS analog integrated circuits. In order to understand the particularities of this domain, attention must be paid to

i) The MOS device physics and the influence of device fabrication on device characteristics

ii) The technology of integrated circuit (IC) fabrication

iii) The characteristics of elementary transistor and MOS connections such as emitter-coupled pairs and MOS source-coupled pairs

iv) Current sources and active loads

v) Output stages and methods of delivering output power to a load

vi) Operational amplifier design

vii) Frequency response of ICs

viii) Analysis of feedback circuits

ix) Stability of feedback circuits

Taking all these into consideration, the final target of this investigation was set up to build stray insensitive switched capacitor composite operational amplifiers, with the purpose of implementing the circuits using a VLSI process. The first time that such an effort was realized was in reference 14.

The initial integrated chip was tested after fabrication, had several problems such as considerable latchup and a difficulty to obtain a noise-free signal at the output. This was estimated to be due to the amount of noise injected into the analog signal path from the digital portion of the circuit.

The results of this first efforts were useful for the understanding of the difficulties that occur in an analog-digital chip that may not be obvious or annoying in a pure digital design. Since the progress only occurs from the good analysis of previous experiments , all of these factors will be taken into consideration for the design of a third generation improved analog-digital chip on two different circuits.

The areas of concentration for the improvement will be :

(1) Effort to have n-substrate and p-substrate contacts in every MOS device

In any case, the n-well should be hard wired (via n+) to power, so that any injected charge is diverted to Vdd via a low resistance path. These measures intend to reduce the latchup and the body effect.

(2) Effort to reduce the spread of the clock pulses into analog areas, which cause distortion to the amplification of the input signals and blur the output.

This was achieved using double guard rings (P+ and N+), in the

design. The P+ will be connected to Vss and the N+ will be connected to Vdd. This way, for example, the P+ collects hole current thereby shielding the N+ source-drain connection.

(3) Effort to reduce the total number of interconnect lines on the chip, aiming to reduce the routing capacitance and the effects of fringing fields.

(4) Effort to obtain a more accurate simulation of the chip, especially checking every single building block hierarchically, going from the simpler to the higher subcells.

The final simulation of the composite amplifiers in *SPICE* will intensively come from the "*MAGIC EXTRACTOR TO SPICE*" software tool and not from a cascaded building of circuits, whenever possible. Thus, multiple interlayer capacitance will be included, which otherwise would not appear. The digital parts will be simulated with *ESIM*, the provided digital simulation software tool, to verify their expected logic.

D. THE MOSIS LOW NOISE N-WELL ANALOG PROCESS

In general, there are many different CMOS manufacturers, that can provide a wide range of technologies to chose from. The technology is usually referred to by the length of the smallest transistor gate that can be produced with that process. Other variations on manufacturers include those that produce only a certain application microchip or those that provide some design flexibility in what is called a semi-custom microchip, or those that provide the most design flexibility in what is called a full custom microchip. [Ref. 14 : pp. 23]

MOSIS was the manufacturing process available for the fabrication of the microchip designed in this thesis. The production line available was a 2 micron technology, full custom process. As it is defined before, that means that the minimum sized transistor has a gate length of 2 microns and that the design could be anything that would not violate the technology design rules and would fit within the area of the microchip. Thus, this process allowed for the maximum amount of flexibility within the limits of technology. It must also be mentioned that there were two layers of metalization available, called metal 1 (m1) and metal2 (m2), two polysilicon layers poly1 and poly2, (necessary for higher precision capacitors, or as the gate of transistors and for short interconnects). PMOS and NMOS transistors were available to implement the CMOS logic, a p-type

substrate with n-wells and for this design a maximum chip size of 2250 microns by 2220 microns.

What makes the process used specific for analog integrated circuits is the fact that MOSIS specifies different fabrication parameters used (they will appear in *SPICE* simulation files), which are meant to introduce less noise in the analog circuit (It must be mentioned that noise is more crucial to an analog circuit than a digital circuit, because anything in the input is transferred to the output, while digital logic is represented only by ones and zeros through threshold voltages that allow some acceptable noise margins). The analog fabrication parameters used are listed in Appendix B.

E. EXTERNAL DESCRIPTION OF THE CHIP, FLOORPLANNING

The chip that is to be constructed has an allowable surface of 4,995,000 μm^2 and maximum of 40 pads. It has been decided to include two single op amps which will be able to be tested independently for comparison reasons. The VLSI software *MAGIC* has been used to implement all necessary components of the microchip. The first step of the design was to decide the use of the available pads. Thus, their use is distributed as follows

(1) **Two pads for analog Vdd and two pads for analog Vss** that supply power to all the bond pads.

(2) **Eight pads reserved for the programmability part** of the chip. These are input pads and their code name inside the chip will be S1x (where x = 0,1,2,3) for TSI C2OA-1 composite OA, and S2x for MOFR C2OA-1.

(3) **Two pads for analog Vdd and two pads for analog Vss** for the analog parts of the chip (where Vdd = +5, Vss = -5 Volts).

(4) **Four output pads,** each one for one amplifier. Their names are out1 for TSI C2OA-1, out2 for MOFR C2OA-1, out3 and out 4 for the two identical single OAs.

(5) **Eight analog pads for the inverting and non-inverting inputs** respectively of the amplifiers. Their names (+) and (-) V1

for TSI C2OA-1, (+) and (-) V2 for MOFR C2OA-1, (+) and (-) V3 and V4 for t' 'wo single amplifiers.

(6) **Four analog output pads for the two phases** (each phase divided into odd and even) **of the non-overlapping clock.** Their names Φ1 , Φ2 and the inverse.

(7) **One digital Vdd and one digital Vss pad for the digital part** of the design.

(8) **One master clock input pad** , named CLK.

(9) **Four internal test point analog pads** for the composite amplifiers. The V11 corresponds to the internal test point # 1 of Figure 6.3 and the V12 corresponds to the internal test point #2 of Figure 6.3. The V21 corresponds to the internal test point #1 of Figure 6.4 and the V22 corresponds to the internal test point # 2 of Figure 6.4.

(10) **One universal ground pad** ,called GND.

In Figure 7.2, one can see the relative placement of the pads inside the pad ring, as well as the position of the composite and single amplifiers. This is called floorplanning, and is defined as the exercise of arranging blocks of layout within a chip to minimize area or maximize speed. The complete microchip layout geometry, as submitted for fabrication, is shown in Appendix C, Figure ApC 1.

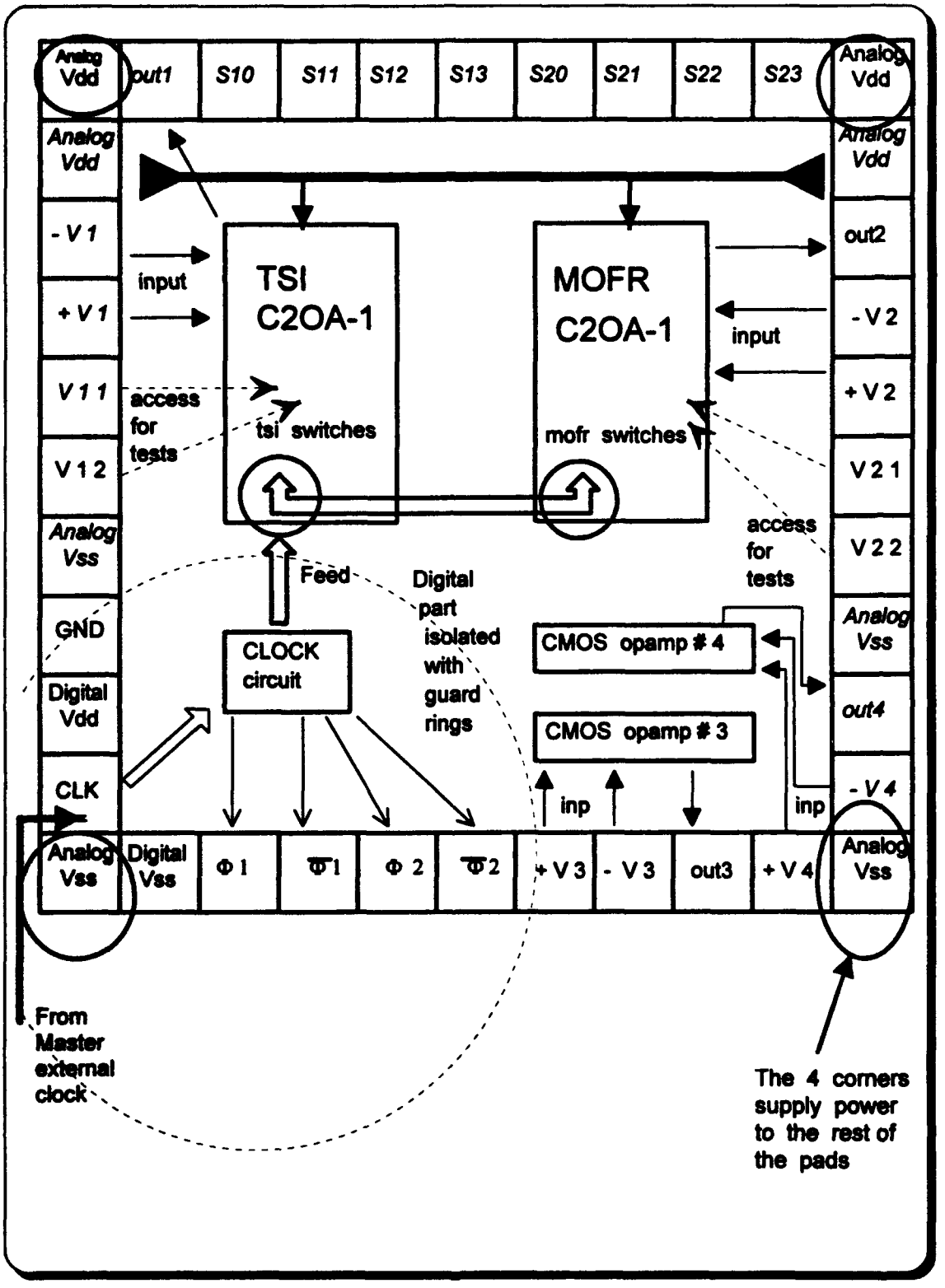


Figure 7.2 Ghost Chip : Floorplan And Bond Diagram

F. DESIGN OF REQUIRED PROGRAMMABLE CAPABILITIES

First, we must say that what will be stated for the TSI configuration will be the same for the MOFR configuration. The programming pins for the TSI C2OA-1 are labeled S13 , S12 , S11 , S10. The pins will use positive binary logic to select the value of the ratio alfa for the composite. Table 7.1 reveals the binary code and value of alfa that is selected. Important for this circuit is the fact that the logic one is +5 Volts, the logic zero is -5 Volts, and the switches close on a logic 1 and open on a logic 0.

TABLE 7.1 BINARY CODING OF THE CAPACITOR RATIO

Capacitor Ratio value (α)	S13 pad input	S12 pad input	S11 pad input	S10 pad input
1	0	0	0	0
2	0	0	0	1
3	0	0	1	0
4	0	0	1	1
5	0	1	0	0
6	0	1	0	1
7	0	1	1	0
8	0	1	1	1
9	1	0	0	0
10	1	0	0	1
11	1	0	1	0
12	1	0	1	1
13	1	1	0	0
14	1	1	0	1
15	1	1	1	0
16	1	1	1	1

This variable capacitor ratio will be changed through the choice of capacitor groups connected in parallel, as it is described in references 1, 10,14 and 22. In Figure 7.3 we can see how the parallel groups are going to withstand inside the chip and give the desired result. The layout geometry of this realization is shown in Appendix C, Figure ApC 2.

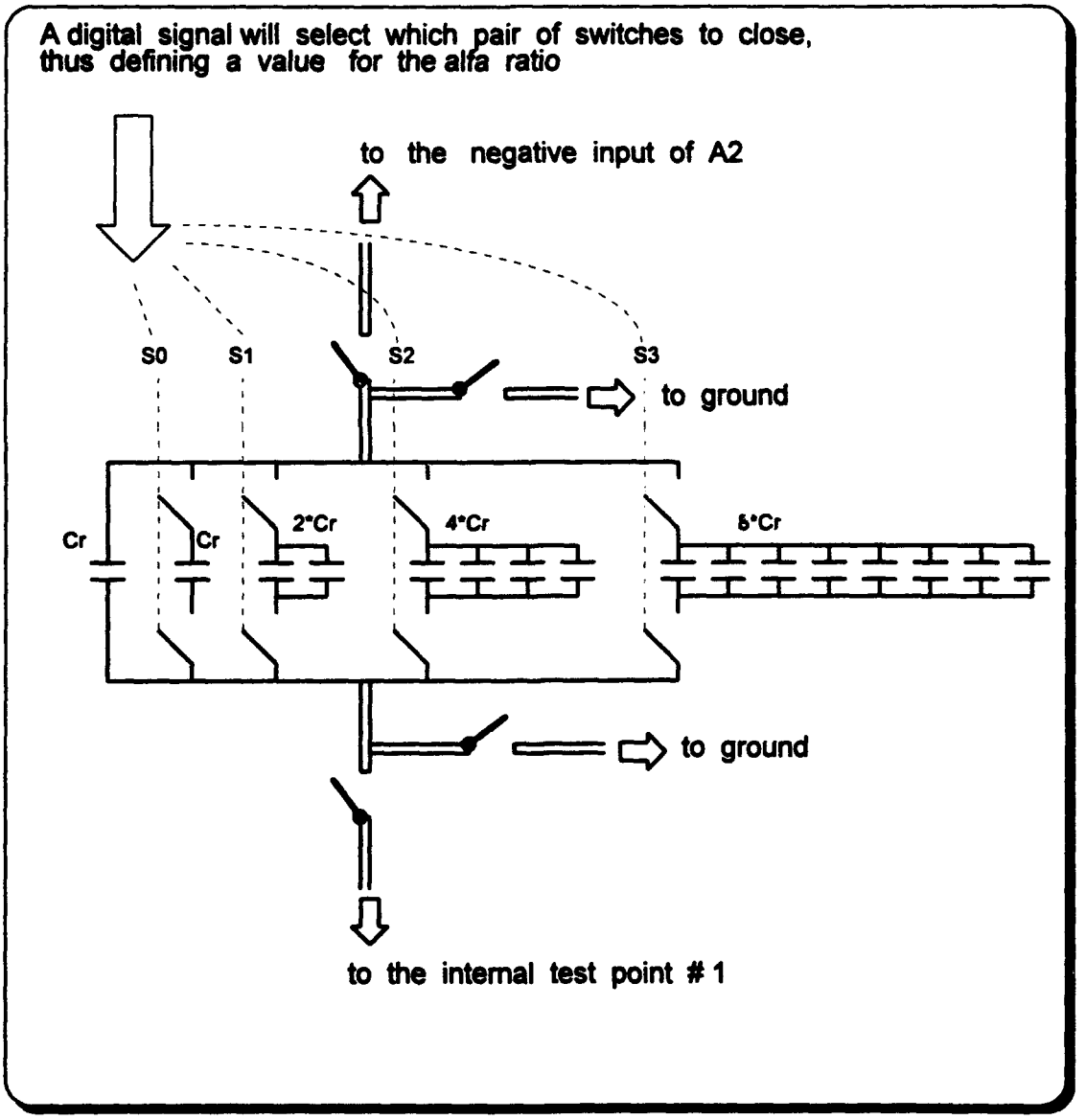


Figure 7.3 Schematic Diagram of the Programmability Part

G. THE CHOICE OF A CMOS OPERATIONAL AMPLIFIER

The most complicated and most important component needed to implement the C2OA-1, in both configurations, was the operational amplifier. A lot of research has occurred in references 9, 10, 14, and 15. The debate was about which OA would give the best results. It has been decided to adopt the one that was found to be the best in reference 14, with the only difference that its performance would be reevaluated in *SPICE* using the latest and more accurate low noise parameters, in comparison with these that were used in reference 14. Its schematic diagram is shown in Figure 7.4.

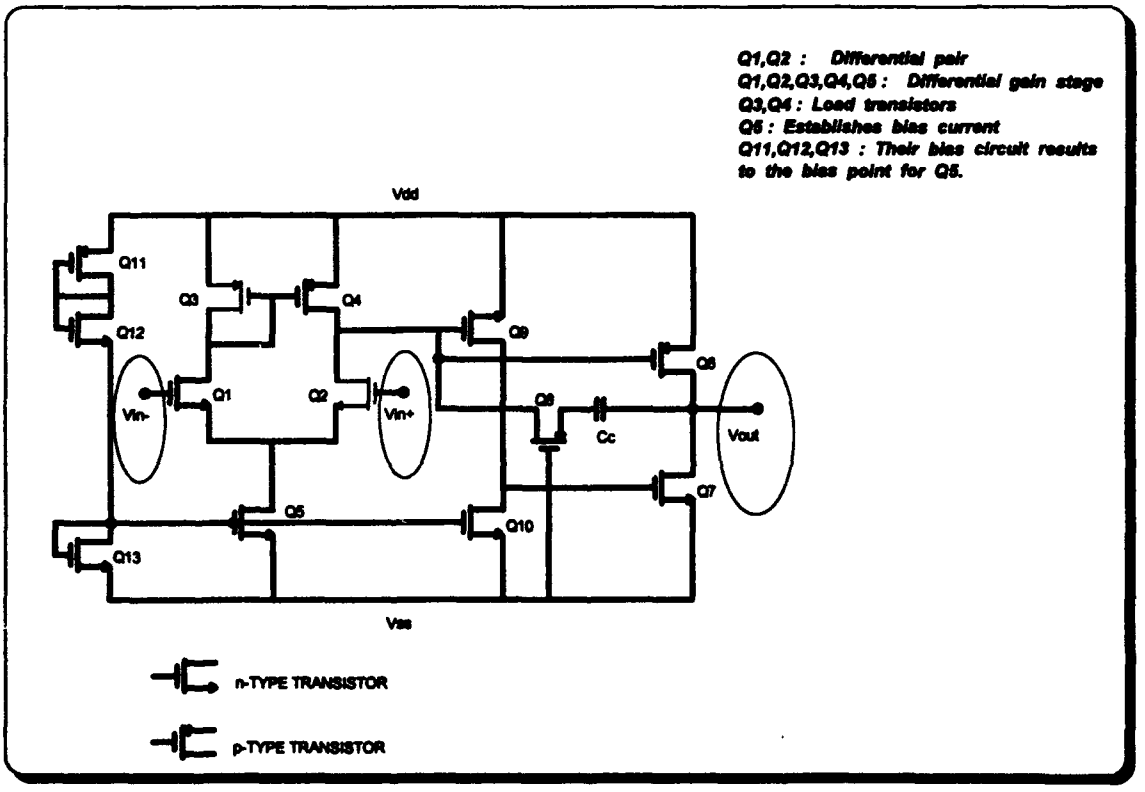


Figure 7.4 CMOS OA Selected Circuit Diagram

As one can see from the circuit diagram, the bias current is established by Q5 and the bias point for Q5 is the result of the bias current created by Q11, Q12 and Q13. This particular bias arrangement was done so as to allow for dynamic Vss and Vdd, that is, the proper bias point was insensitive to changes in the voltage supplies. The differential gain stage made by Q1, Q2, Q3, Q4 and Q5 is a differential input but a single ended output. The single ended output feeds into Q9 and Q6. Q9 in conjunction with Q10 provides level shifting and an additional gain stage. Q8 and the compensating capacitor provide feedback that maintains the stability of the amplifier. Q6 and Q7 provide a class-AB output stage, similar to a totem pole driver stage in bipolar technology. The advantages of this circuit are the internal compensation and an internal bias circuit which results in fewer internal pins. It can also drive a larger load because of its dedicated output stage [Ref. 9 : pp 168 - 245].

The analog process was helpful to the fact that the size of the compensation capacitor was kept small because of the use of the poly1 to poly2 capability. Thus the transistors of the amplifier were relatively big, providing a high open loop gain as well as a high load capability. There were guard rings around the differential input transistors, as well as around the transistors acting as current sources for the gain stages. The layout implementation is shown in Appendix C, Figure ApC 3.

H. THE TWO PHASE NON-OVERLAPPING CLOCK

The two phase non-overlapping clock is built using a latch, and then placing multiple inverters in the feedback path that controls when and for how long a switch is opened and closed.[Ref. 9 : pp 516 - 518] The allowance of the even inverted non-overlap is in the nanosecond range, as it will be shown later in the simulation, thus the design is absolutely safe. The number of inverters used is the one that defines the delay introduced. In Figure 7.5 we can see its schematic diagram, in Figure 7.6 the transistor level diagram, and In Appendix C, Figure ApC 4, the layout geometry.

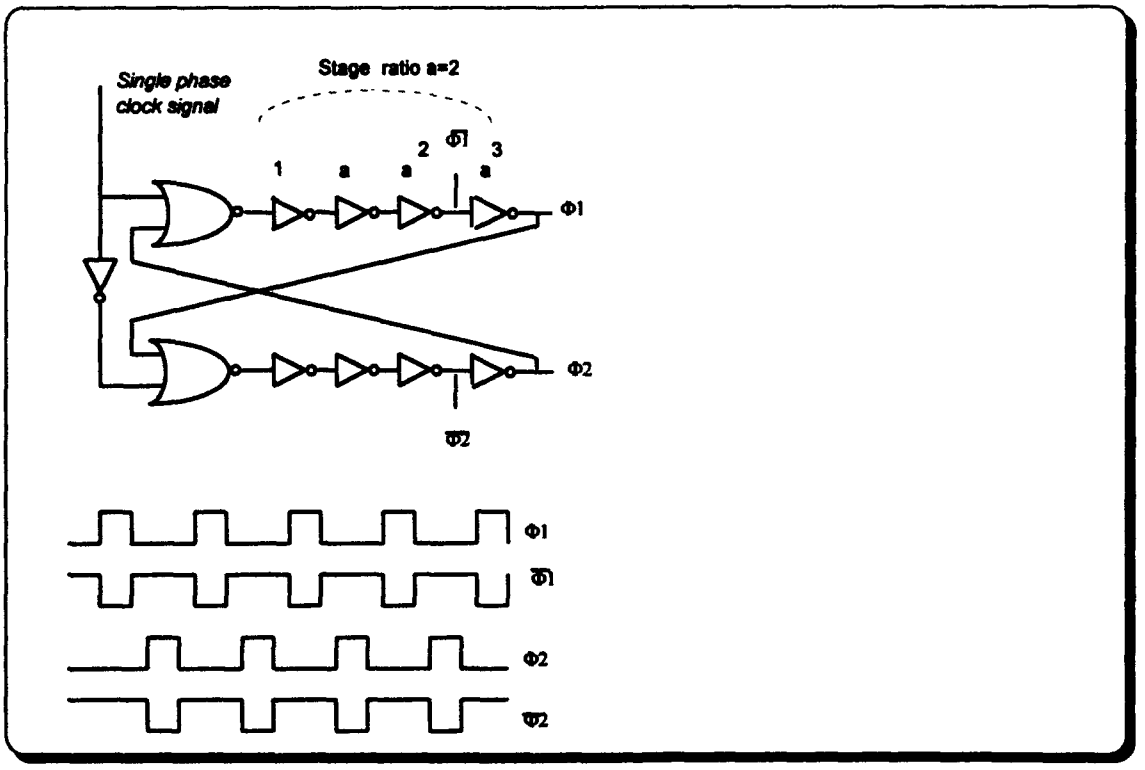


Figure 7.5 The Two Phase Non-Overlapping Clock Circuit Diagram

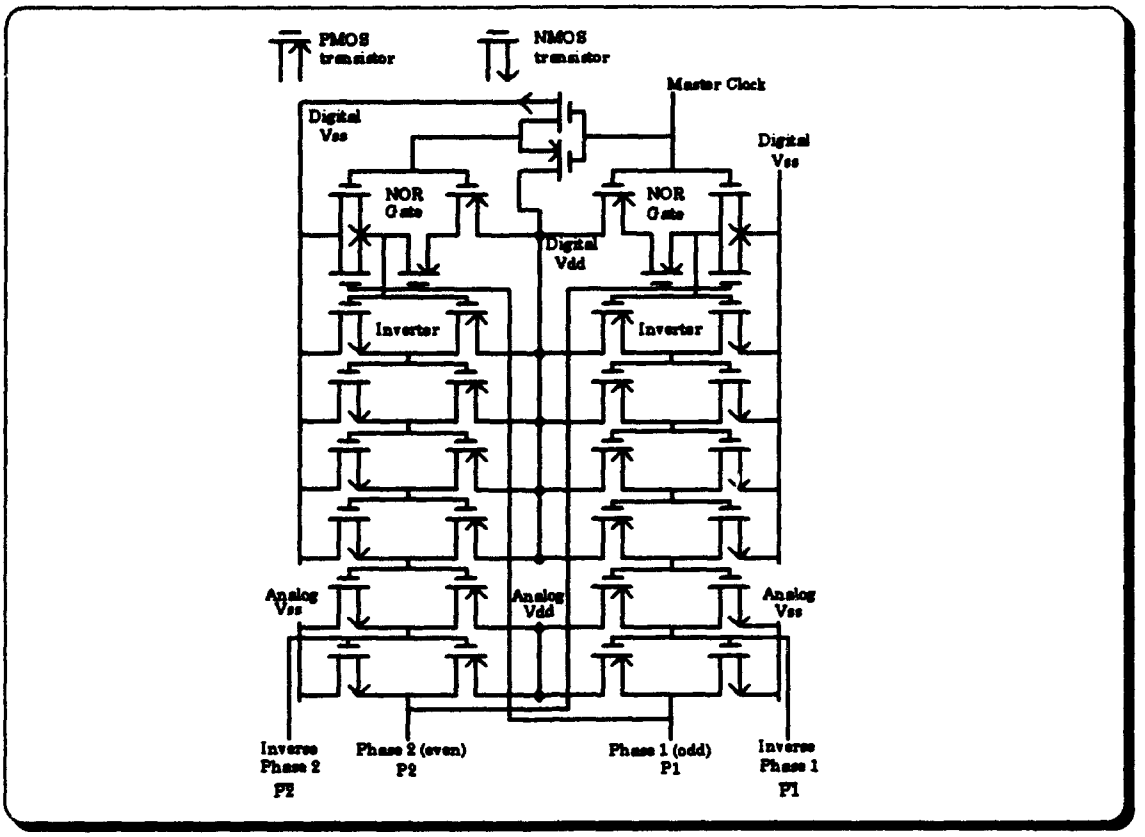


Figure 7.6 Transistor Level Circuit Diagram for the Clock Used

The layout geometry of the subcells used for the clock implementation, the 2-input-NOR gate and the inverter, are shown in Appendix C, Figures ApC 5 and 6.

I. THE TRANSMISSION GATE

The gate controls the passage of current between the source and the drain. Simplifying this to the extreme allows the MOS transistors to be viewed as simple on-off switches. There is some peculiarity though, a N-SWITCH is almost a perfect switch when a zero is to be passed from an

input to an output, but an imperfect switch when passing a one. The opposite happens to a P-SWITCH. By combining an N-SWITCH and a P-SWITCH in parallel, one obtains a switch in which zeros and ones are passed in an acceptable fashion. We term this a complimentary switch, or C-SWITCH, or transmission gate in our case. Its schematic diagram is shown in Figure 7.7 and its layout geometry in Appendix C, Figures ApC 7 and 8.

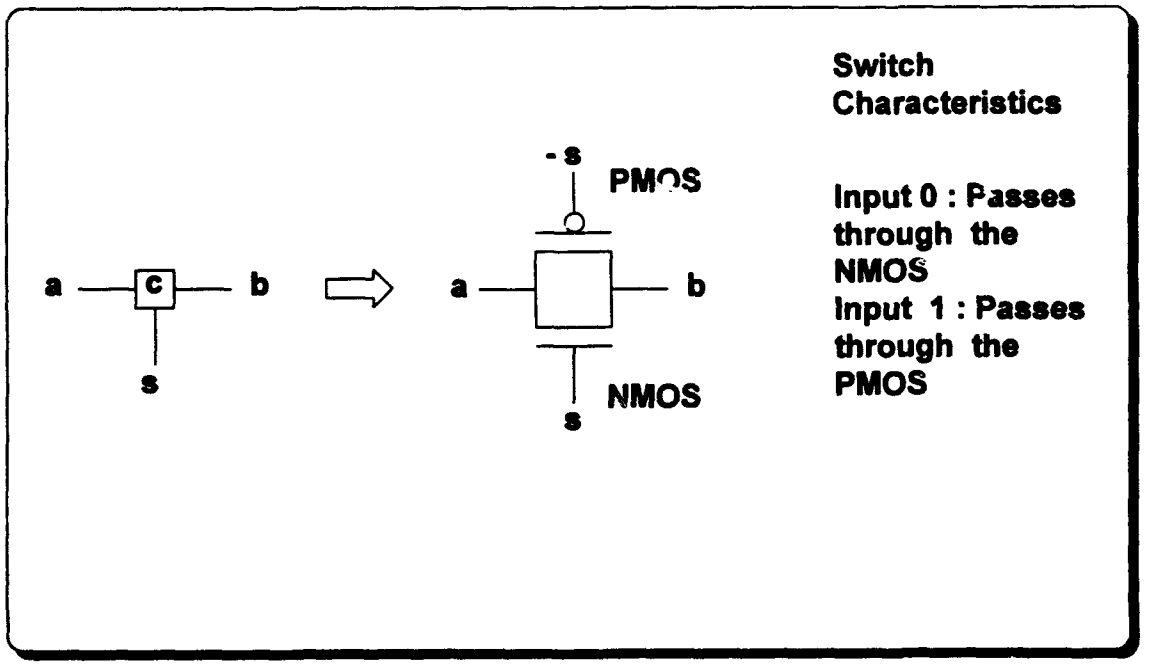


Figure 7.7 Complementary Transmission Gate

There are some non-ideal characteristics in the design of the transmission gate that must be considered. These are the parasitic capacitances associated with transistors and the on-channel resistance which is in the range of several KΩ and influences the signal that passes. Equation 7.1

defines the variation parameters of the on-channel resistance

$$R_C = \frac{1}{\mu * (\frac{\varepsilon_0 * \varepsilon_r}{t_{ox}}) * (V_{gs} - V_t)} * \frac{Length}{Width} \qquad (7.1)$$

where μ = surface mobility

ε_o , ε_r = The dielectric constants of the insulating layer

t_{ox} = The thickness of the oxide or insulating layer

V_{gs} = The gate to source voltage of the transistor

V_t = The threshold voltage of the transistor

It is obvious that the designer can only control the width and length of the transistor. The ways to reduce the on channel resistance are either to reduce the (length/width) ratio, or connect two transmission gates in parallel [Ref. 14 :pp 50]. In several simulations, different ratios had been tested, and the final on-channel resistance varied between 82 Ω and 141 Ω for the range -5 to 5 Volt.

J. CONNECTING ALL PARTS TOGETHER : THE COMPOSITE OA

The only remaining design task, was to connect all the parts described, in order to implement the two different configurations of the composite amplifier and also provide all necessary lines that lead to the scheduled pads. In order to reduce the lines that were to feed the circuit with Vss and Vdd, a handy idea was realized. Since the two guard rings(P+ and N+) that surrounded the composite would be in real Vss and Vdd voltage

respectively, and also a metal line would pass underneath to power the substrate contacts, we could use this metal line to bias the amplifiers with a very small extension where necessary. The use of double guard rings for a p-substrate is shown in Figure 7.2.

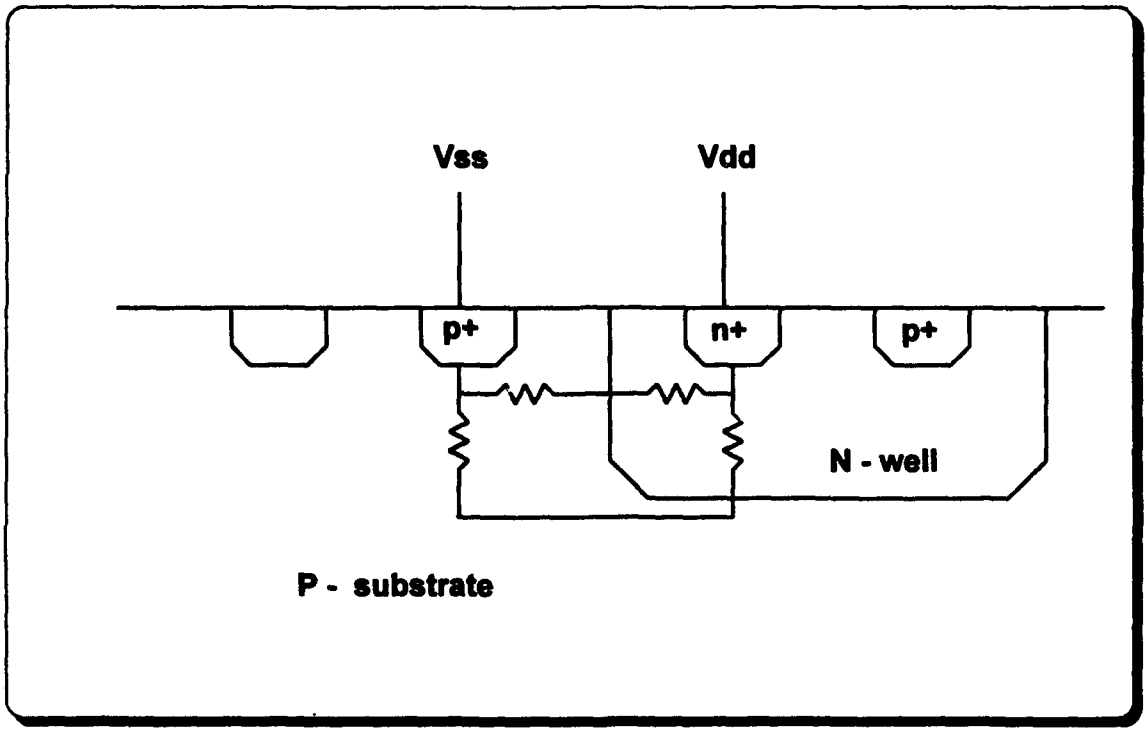


Figure 7.2 The Use Of Dummy Collectors To Reduce Latchup

The final schematic diagram is shown in Figure 7.3 for the composite C2OA-1 with MOFR damping and in Figure 7.4 for the TSI damping. The layout geometry is shown in Appendix C, File ApC 9.

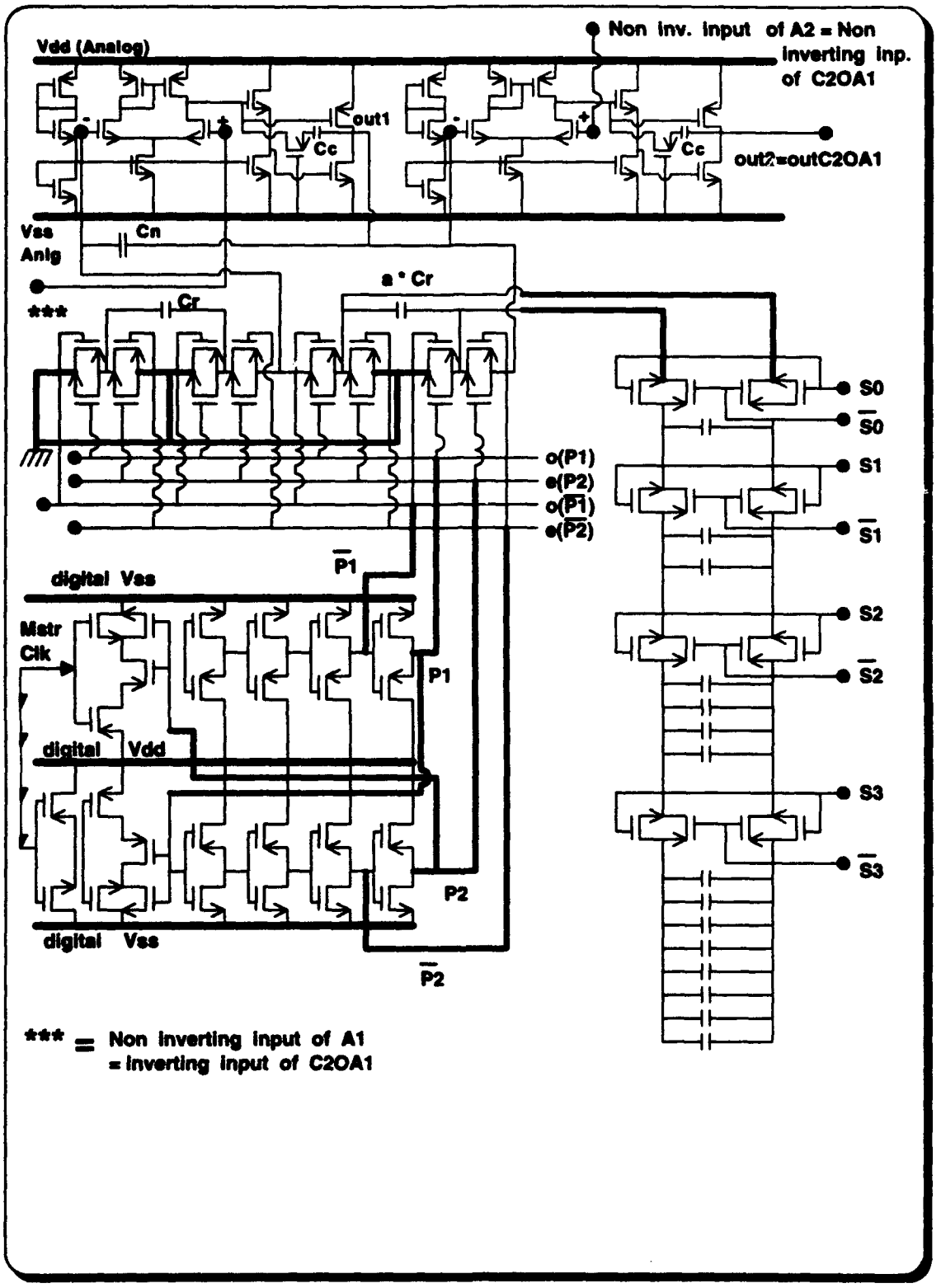


Figure 7.3 Complete C2OA - 1 : TSI Damping

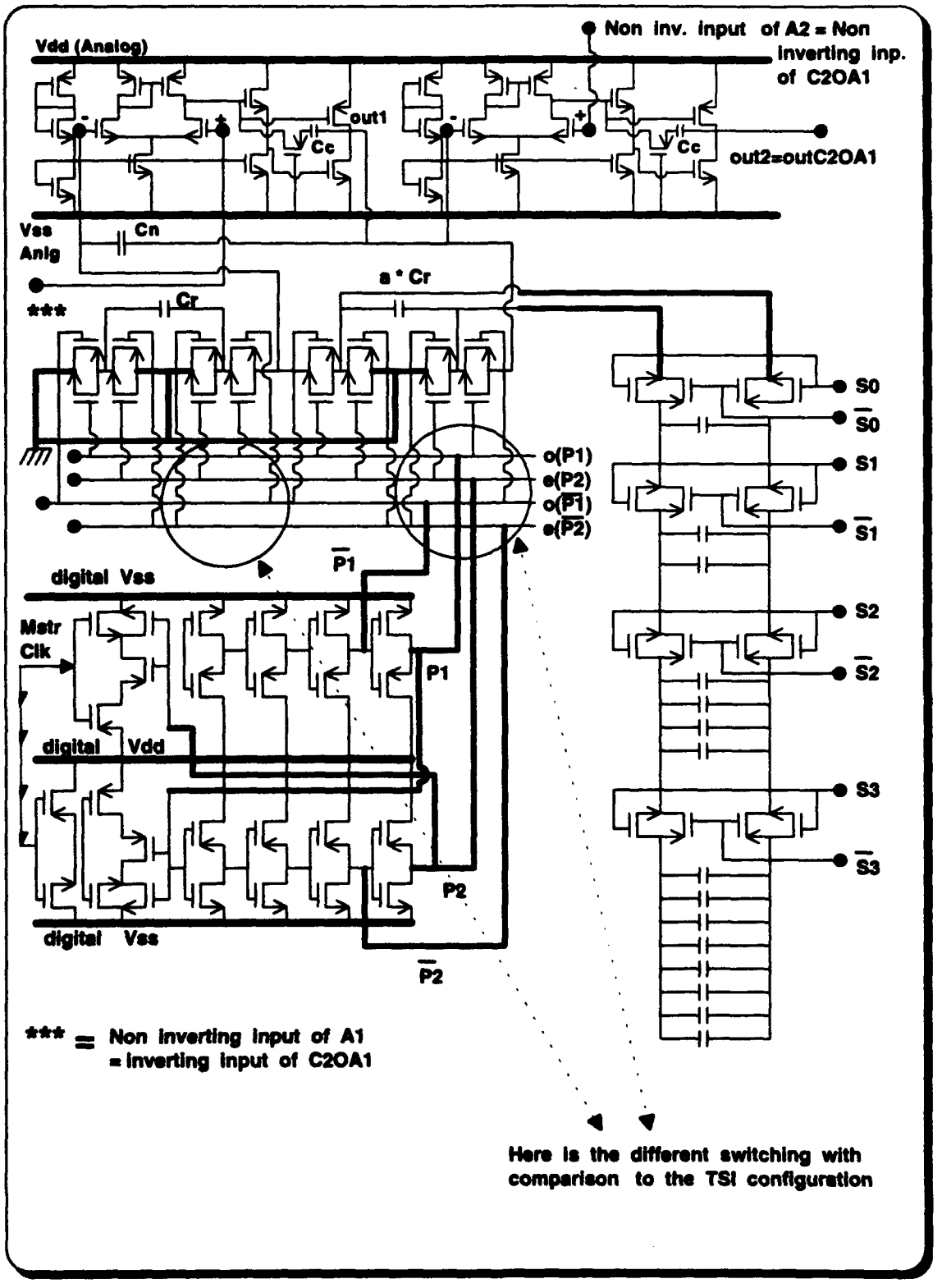
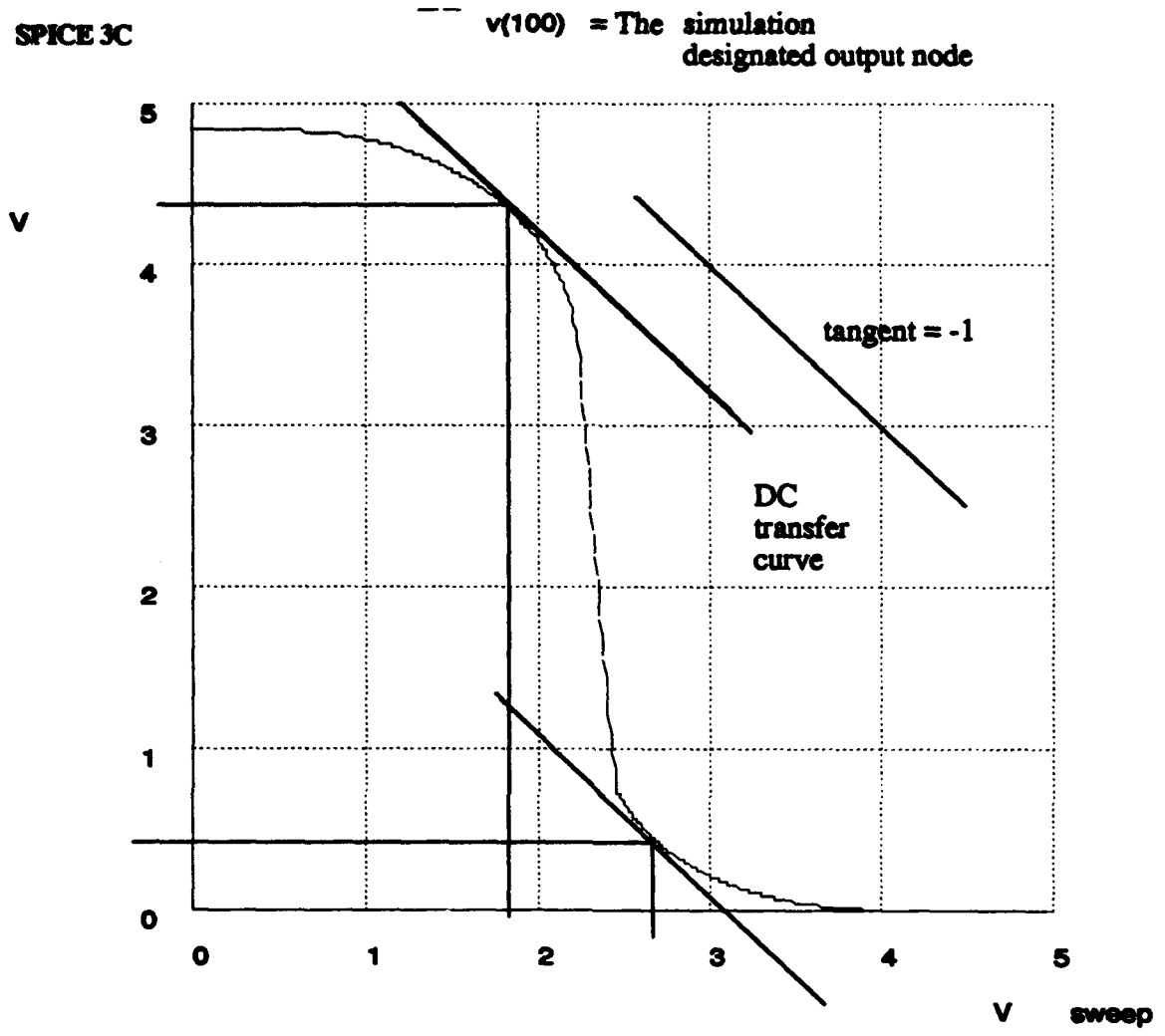


Figure 7.4 Complete C2OA - 1 : MOFR Damping

K. SIMULATION AND TEST RESULTS

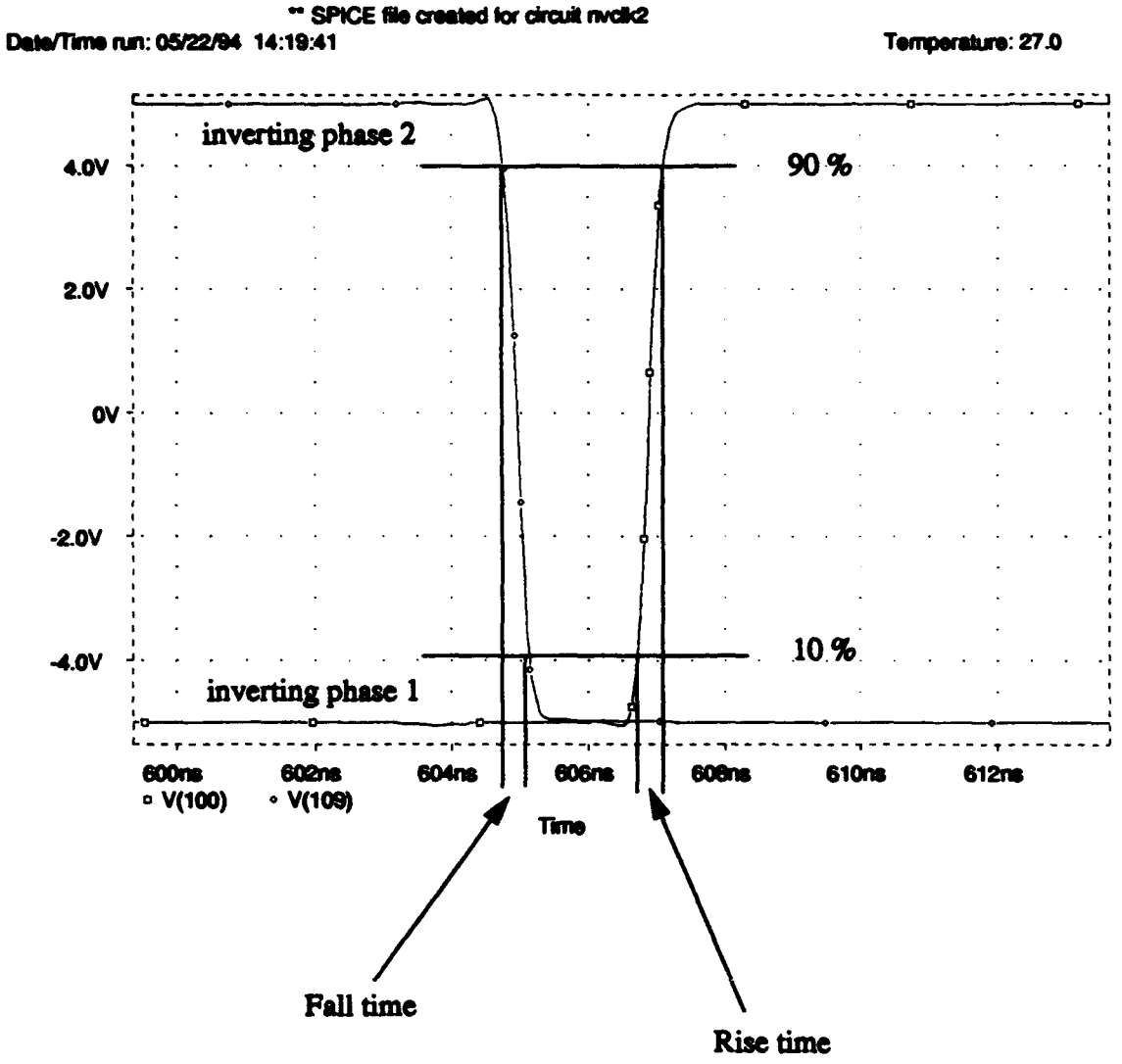
All digital magic cells such as the inverter, the transmission gates, and the two phase non-overlapping clock were simulated using the event driven logic-level simulator *ESIM* to verify performance of the required functions. In addition, to determine the resultant pulse width and delay for the one shot, *SPICE* was used to perform transient analysis. The simulations are listed in Appendix D, Files C, D and E. The single CMC operational amplifier, as well as the composite amplifier, were simulated only by *SPICE*. This program was sufficient to provide all necessary information to the single amplifier, but not to the composite amplifier. In the last one only a transient analysis plot was realizable, but not any frequency response plot which would also provide power consumption information. The appropriate software to test the switched capacitor composite amplifier would be *SWITCAP*, which was not available. Still, the obtained transient analysis results matched the ones that were found from the mathematical analysis of the circuit, giving serious belief that the implementation this time would be successful. To avoid redundancy of simulation results, only the plots of the inverter's DC curve, clock's and composite amplifier's transient analysis (100 KHz and 350 KHz), and CMOS amplifier's frequency response will be shown in Figures 7.5 through 7.9 respectively.



Comments : The used circuit logic is :
True : + 5 Volts
False : - 5 Volts
The noise margins are sufficient
This is the first out of 3 different ratios (width / lengrth) inverters that were used in the clocking circuit

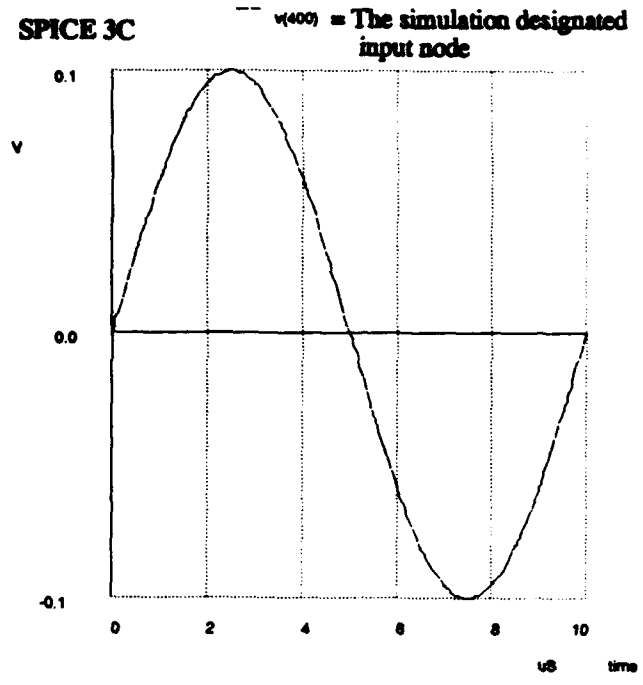
NM low = 1.5 Volts
NM high = 1.7 Volts

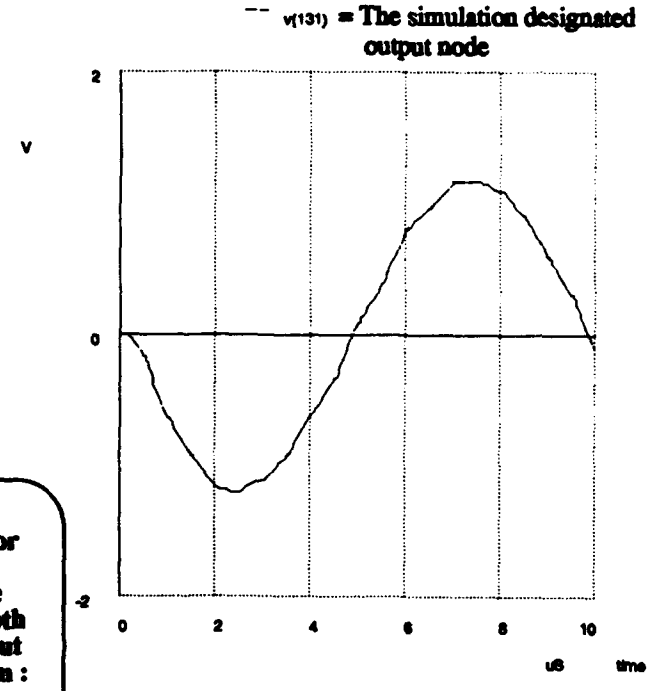
Figure 7.5 The Inverter Cell DC Analysis Plot



Comments : 1. The rise time is longer than the fall time as expected
2. The non - overlapping time gap is sufficient for this application. It is controlled by the number of inverters in series used.

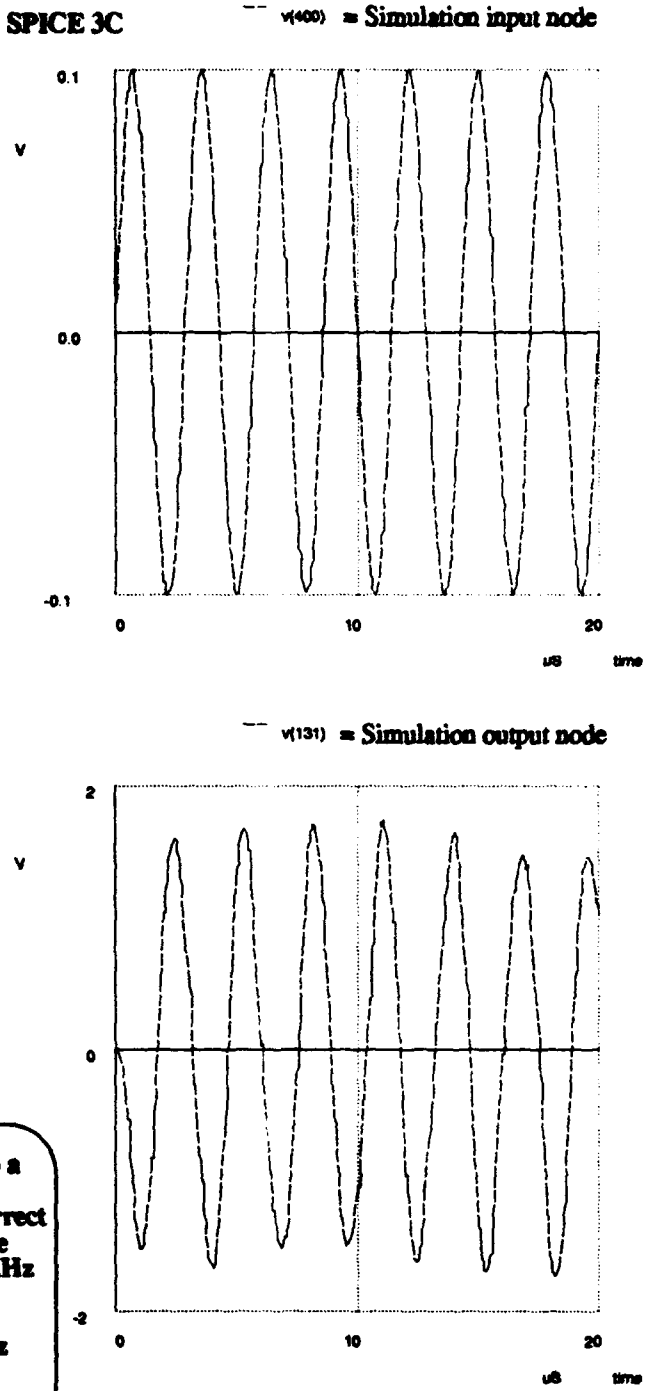
Figure 7.6 The Two Phase Non Overlapping Clock Transient Analysis





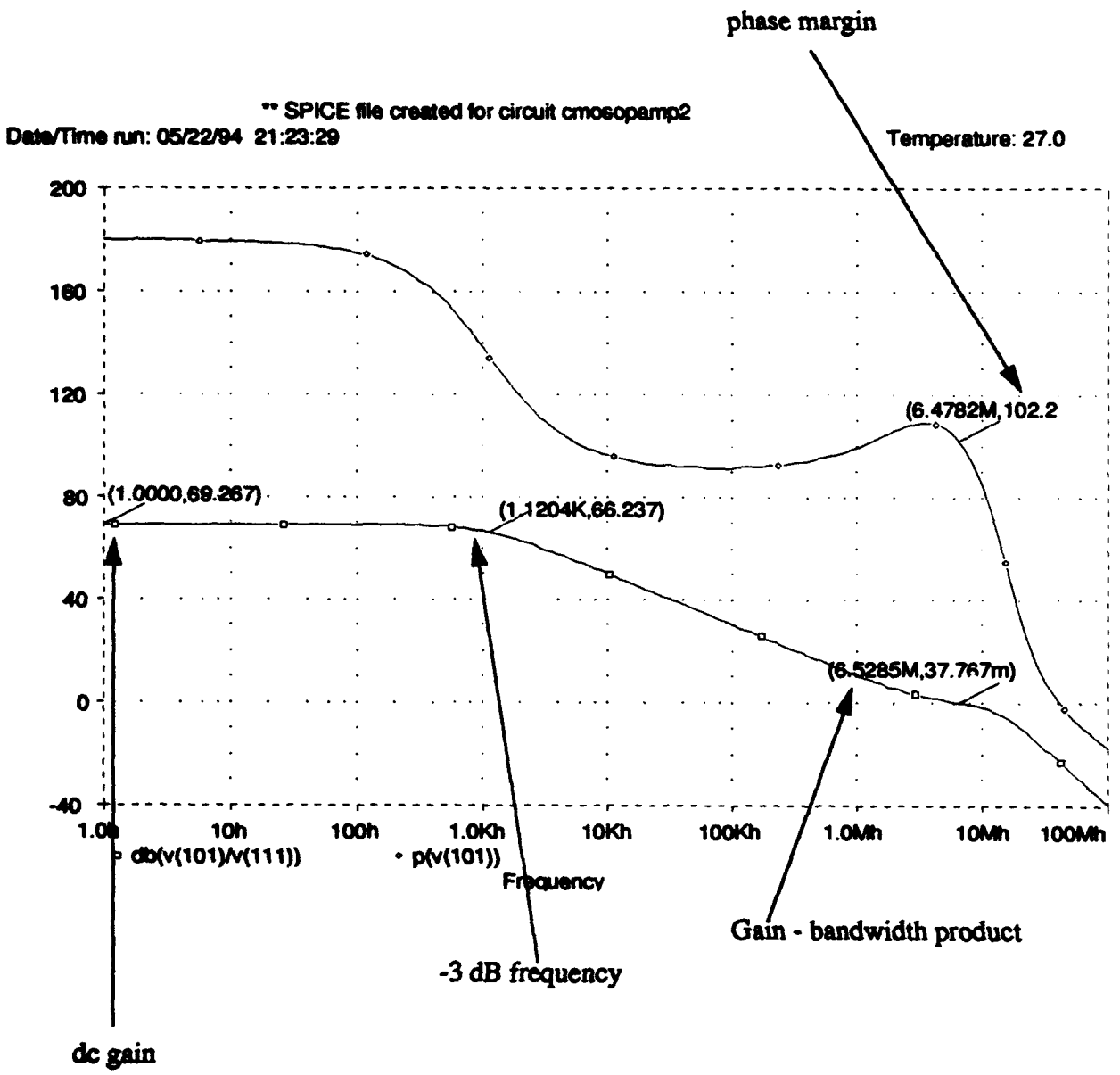
Comments : The feedback capacitor C_F role is very important for the regular and smooth shape of the output
Final value chosen : 6 picofarad
This application : Negative gain - 10

Figure 7.7 The C2OA - 1 Composite Amplifier : Sinusoidal Steady State Response For 100 KHz Input



Comments : Even to a high frequency the output is close to correct
Reminder : Since the sampling rate is 1 MHz the maximum input signal cannot be higher than 500 KHz for anti - aliasing reasons
Negative gain : - 100

Figure 7.8 The C2OA - 1 Composite Amplifier : Sinusoidal Steady State Response For 350 KHz Input



Comments : In comparison with a bipolar operational amplifier we have less dc gain but better GBWP and a better phase margin

Figure 7.9 The Analog CMOS Operational Amplifier : Frequency Response Information

L. CONCLUSIONS

The *SPICE* simulation results have shown an approach toward the success of the chip that is going to be fabricated. The simulations are not the "blind guide" though, because in the actual fabrication we may have imperfections such as non vertical lithography, or bad doping which is not anticipated by *SPICE.* Also, we do not have all detailed information that only a software program designated exclusively for switched capacitors, such as *SWITCAP*, would give. The individual results for the single amplifier, the clock, and the elementary building blocks are of maximum possible accuracy and encourage the confidence that they were not away from reality. The important is that according to the simulations, we get a proof of correct concept that matches the mathematical foundation of the microchip.

VIII. APPLICATIONS

A. WHERE AND WHY THE USE OF NEURAL NETWORKS

The current explosion of interest in artificial neural systems is based on a number of scientific and economic expectations. One should be aware, however, that some of the popular expectations may be exaggerated and are not realistic. We can be quite sure that neural networks will not replace conventional computers. The two main reasons are, first the low cost of the conventional digital computers, and second the fact that these so far outperform any other computing devices in numerical calculations.

One possibility for the use of artificial neural systems is to simulate physical systems that are best expressed by massively parallel networks. Also, low-level signal processing might be best done by parallel analog or analog and digital neural networks. Perhaps the most likely applications for neural networks will be those involving classification, association, and reasoning rather than sequential arithmetic computing. It seems that the areas requiring human-like interface perception of speech and vision, whenever the real time parameter is needed, are the most likely candidates for applications. Neural networks are also expected to be widely applied in expert systems and a variety of signal processors. At present, such systems are available as aids for medical diagnosis, financial services, stock price prediction, solar flare forecasting, radar pulse identification, and other

applications. As most researchers agree, future artificial neural networks are going to offer a complimentary technology to the purely digital one. The ultimate goal may be to exploit both technologies under the same roof, while presenting a single, flexible interface to the user. [Ref. 17 : pp 1 to 22]

B. RELATION OF THIS IMPLEMENTATION

This is exactly the philosophy of the chip that has been fabricated, combining analog and digital advantages. It belongs to the nature of the switched capacitor circuits to require a thorough knowledge of technology and an understanding of the kind of applications that these will enforce. The anticipated purpose of this microchip implementation is to attract even more research in the VLSI neural network implementation, ultimately offering solutions to the following domains

1. Engineering

Applications in this field would envolve combining high information accuracy, and low weight, coupled with extreme speed and complex image processing capabilities. Image processing in this case includes image classification and interpretation. The term "images" applies to all two-dimensional patterns, not only to the visual images. The following list names all domains and applications where use of neural networks is recommended

a. Image processing

Applications : Motion, color, depth

b. Image interpretation

Applications :Fault detection, classification, counting, optical path tracking

c. Optimization

Applications : Routing, placement, 2D cost function

d. Solving nonlinear partial differential equations in real time

Applications : Navier - Stokes equation used in weather prediction

e. Simulating nonlinear waves

Applications : Solitons, autowaves, spiral waves

2. Neurobiology

Most neurobiological systems are comprised of two-dimensional neural array processors consisting of locally connected neurons. Neurobiologists need a standardized structure upon which to attach the vast store of information available from experimental data. Programmability is required for this kind of applications.

a. Sensory systems

Applications : Vision, Audition, Olfaction, Taste, receptor arrays, cortical processing of sensory information

b. Motor systems

Applications : Cerebellum, ocular motor system, sensory-motor association areas

3. Consumer electronics (List of most commercial features)

(1) Smart video camera that adjusts for brightness, color constancy, contrast, motion, even in local regions of the visual scene

(2) High speed character recognition

(3) Depth perception

(4) Deblurring functions

(5) Remote processing of medical images

(6) Classifying and analyzing auditory signals

4. Industry and Physics (List of research fields)

(1) Stress and Heat analysis

(2) Thermographic heat analysis

(3) Super high speed cameras triggered by prescribed events (high energy physics)

(4) Robot vision

(5) Automatic visual inspection in manufacturing

In the next subsection, two specific examples of the composite amplifier hardware implementation, on a neural network application, will be given.

C. BUILDING THE NEURAL PROCESSING NODE

The basic processing unit is defined as the processing node (neuron) and weights (synaptic connections). The processing node needs to memorize data stored as connection weights, to generate a neuron's activation value, and to compute the unit's output signal. These units would make it possible for the unit to perform recall functions. In a simple version, weights can be determined by resistance values, and the analog computation of a scalar product and subsequent non-linear mapping can be performed by a summing amplifier with saturation, as it is shown in Figure 8.1. This operational amplifier can very well be the composite for a high demanding network.

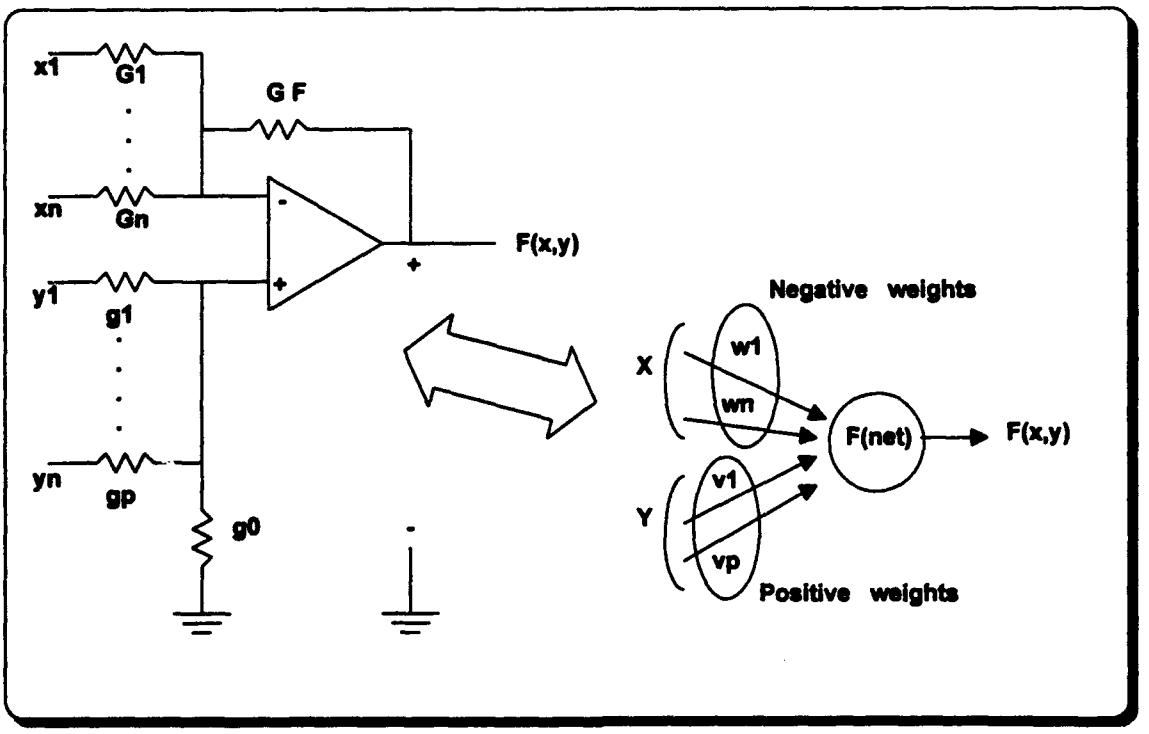


Figure 8.1 Resistor OA Implementation Of Neuron With Weights

The objective is to express the neuron's weight values and its range of linear operation in terms of circuit component values. We assume momentarily that the neuron made of an operational amplifier operates in the linear region. According to the superposition technique, F(x,y) can be computed as the sum of individual n + p responses, which are the results of each separate excitation.

A simple variable input would give

$$f(x) = f(\sum_{j=1}^{n} w_j * x_j) \tag{8.2}$$

The two variable input results to

$$f(x,y) = \left\{ \begin{array}{ll} f_{sat-}, & for\ net < f_{sat-} \\ net, & for\ f_{sat-} < net < f_{sat+} \\ f_{sat+}, & for\ net > f_{sat+} \end{array} \right\} \tag{8.3}$$

where net = $w^{transpose} * X + V^{transpose} * Y$. The activation value net is not measurable or physically present anywhere in the discussed neural computing node circuitry. It is helpful, however, to define and use this variable as a hypothetical input voltage of a unity-gain saturating amplifier.

It is not within the purposes of this investigation to analyze the functions of neural networks, but simply to show that the composite amplifier can provide an enhanced performance when implementing basic neural networks. From the initial assumption that the amplifier operates in the linear region, one can understand why it is an advantage to use the

composite amplifier instead of the single OA, considering its proven improvements in bandwidth and stability.

Another application of a composite amplifier as a summing amplifier can be demonstrated by the following example, that is the design of a missile sensor for military applications. This has to do with the *Expert matrix method.* Although the existing methods of sensor effectiveness evaluation are extremely useful in understanding the workings of a sensor system in a given scenario, they fail to provide a quantitative measure of sensor effectiveness. By using artificial intelligence methods and ideas, *the Expert matrix method* procedure is developed. Using this method and drawing upon experience gained from the scenario method, engagement models, and expert opinions, we can quantitatively improve the sensor effectiveness. The exact equations and the deep understanding of this complicated method is found in Reference 30, pages 284 to 298. The only principle that we need to mention in this investigation, is the fact that we simply need derivation of weights as shown in the weighted summer. This is the solution of a fundamental problem in decision theory, how to derive weights for a set of activities according to their importance. The idea is to initially estimate the matrix of relative weights and then obtain a more accurate estimate by calculating the eigenvector (characteristic vector) of this matrix. One can see that, if the initial assumed relative weight vector is absolutely correct,

then the calculated eigenvector will be identical to it. This is exactly the task demanded by the weighted summer of Figure 8.1, and the fact that it can be implemented in a digital-analog microchip make it suitable for implementation of the sensor system of any military missile. Figure 8.2 and Table 8.1 illustrate a basic theoretical multisensor system that is to be built, and the element weights which need to be determined.

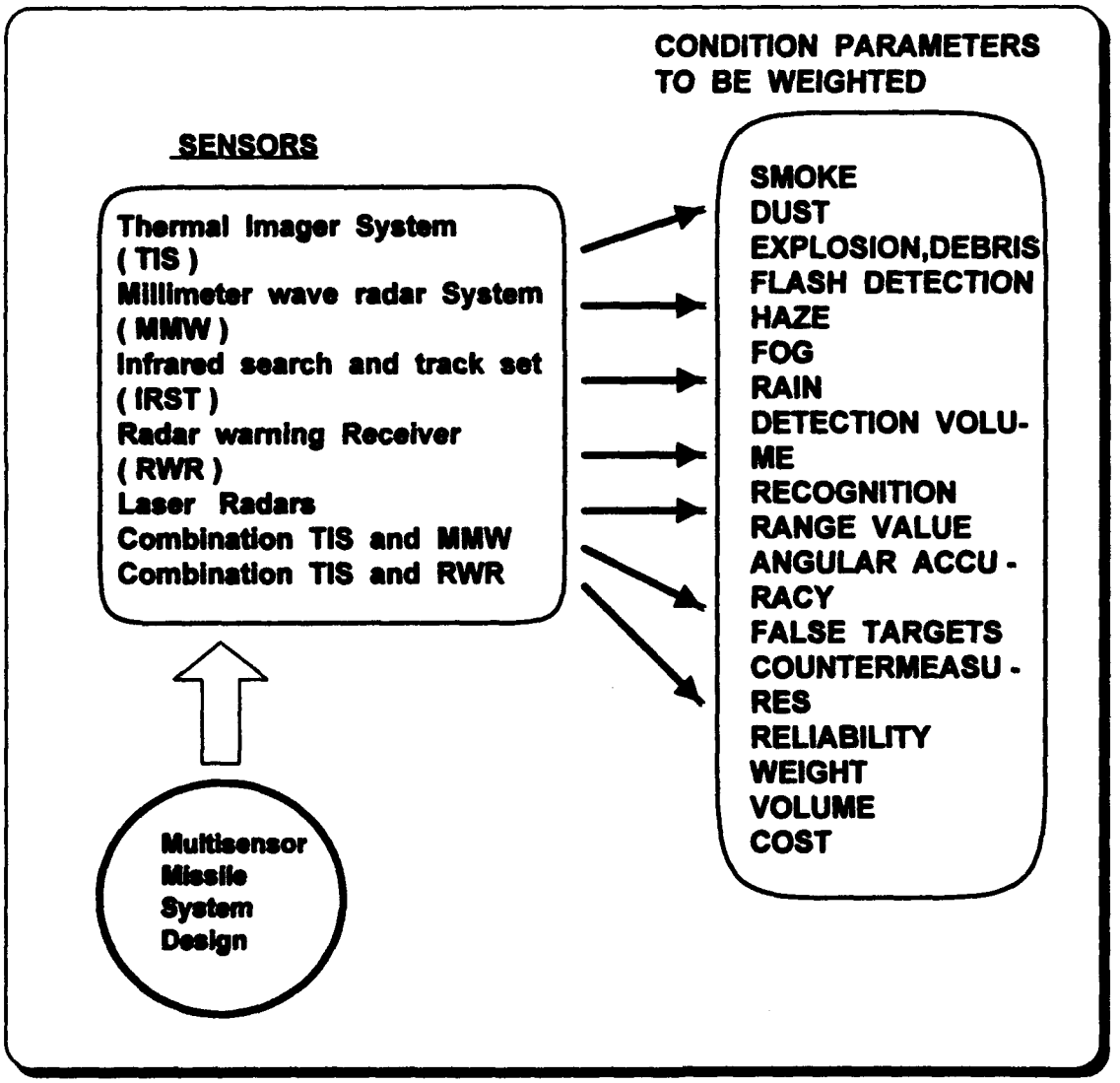


Figure 8.2 Sensors : Operating Conditions and Parameters

TABLE 8.1 SENSOR WEIGHTS MATRIX

Sensor	Smoke Dust	Weather	Search Volume	Recognition	Range value	Angular value	Countermeasure False alarm
TIS	3	5	3	10	5	10	10
MMW	9	9	9	1	9	5	5
IRST	3	3	9	1	1	1	3
TIS & MMW	9	9	9	10	9	10	10
RWR	9	9	3	1	1	1	10

This example demonstrates the general idea of how important the applications of an accurate weighted summer can be, and where the research in analog-digital systems may lead to. One can also understand that sometimes when the accuracy is the main demanding factor on a design, then the analog switched capacitor design of a neural network is the more appropriate way to go.

IX. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

This thesis represented an effort to standardize and justify the steps that lead to the derivation and the VLSI implementation of analog-digital integrated circuits using switched capacitor principles.

It has been proven that a viable mathematical analysis is possible and that a circuit that is first designed in the analog domain using resistors can then be transformed to a new circuit in the switched capacitor domain using equivalent damping models. Using this method, stability and frequency response information can be derived using equivalent z-transform techniques. Proper use of advanced mathematical software packages can minimize the possibilities of errors in the derivation of complicated transfer functions. Thus, anticipation of output results and evaluation of a design can be expected to save time and effort before resorting to hardware and layout implementation or simulation using Spice.

The availability of a VLSI process, optimized for low-noise analog circuits, together with increased emphasis on design considerations such as double guard rings, prevents annoying interaction between the analog and digital parts and minimizes noise injection in the analog signal path. It is also advised that substrate contacts be included in the design for any NMOS and PMOS device at the lowest subcell level.

The scope of this work covers the complete mathematical evaluation of two different switched capacitor topologies applied to the improved design of the composite amplifiers. VLSI implementation, and simulation of this third generation stray insensitive switched capacitor CNOAs, will also be presented. The time was not sufficient to get back and test the fabricated microchip, but the time spent in the most realistic possible simulations provided knowledge and experience. The results and the design may form the basis for an improved future VLSI implementation of artificial intelligence neural systems.

B. RECOMMENDATIONS FOR FUTURE RESEARCH

1) Any switched capacitor design, before it is going to be implemented in a microchip, should be analyzed mathematically, as it is done in the present research. Sensitivity analysis would also be very useful.

2) In order to have more pads available on the chip for external connections, ICs should be designed such that instead of implementing two separate composite amplifiers that differ only in the damping (TSI and MOFR, respectively) only one composite amplifier with programmable damping should be designed.

3) Further improvement of the single operational amplifier used in the design will enhance the overall performance of the composite amplifier. This improvement can be accomplished through the use of BiCMOS technology.

Operational amplifiers implemented using this technology demonstrated a notable enhancement of their characteristics. Future work in this area should consider the use of BiCMOS technology, as soon as design and testing software tools are available at the Naval Postgraduate School

4) Improvements could be made in circuit simulation, especially in the early design evaluations, by the availability of the software package *SWITCAP*. Unfortunately, *SPICE* cannot provide all neccessary information, specifically in the frequency, dc, and ac analysis of switched capacitor networks.

5) After the testing of the current microchip, all working cells can be redrawn in a more compact form. The only way for more capability to be provided within a relatively small area, using the same parameters, is to use tested and proven cells in the tightest possible area management.

```
C2OA1 : MOFR, Ideal Open loop transfer function


Solve[{vout==(va-v1)*A2,
       v1==(vb-v2)*A1,
       (va-v2)*Cr==(v2-v1)*(Cn(1-z^(-1))+a*Cr)},{v1,v2,vout}]
{{vout -> A2*va + A2*(-(A1*vb) -
      (A1*(Cr*va*z + A1*vb*(-Cn + Cn*z + a*Cr*z)))/
      (Cn - Cn*z - Cr*z - a*Cr*z - A1*(-Cn + Cn*z + a*Cr*z)))

X=ExpandAll[vout];
Y=Together[X];
NM=Numerator[Y];
ena=Collect[NM,va];
duo=Collect[ena,vb];
olpideal=duo/Denominator[Y]
(vb (A1 A2 Cn - A1 A2 Cn z - A1 A2 Cr z - a A1 A2 Cr z) +

   va (-(A2 Cn) - A1 A2 Cn + A2 Cn z + A1 A2 Cn z + A2 Cr z +

      a A2 Cr z + A1 A2 Cr z + a A1 A2 Cr z)) /

 (-Cn - A1 Cn + Cn z + A1 Cn z + Cr z + a Cr z + a A1 Cr z)
```

```
C2OA1 : MOFR, Real Open Loop Transfer Function


olpideal=duo/Denominator[Y]
(vb (A1 A2 Cn - A1 A2 Cn z - A1 A2 Cr z - a A1 A2 Cr z) +

   va (-(A2 Cn) - A1 A2 Cn + A2 Cn z + A1 A2 Cn z + A2 Cr z +

      a A2 Cr z + A1 A2 Cr z + a A1 A2 Cr z)) /

 (-Cn - A1 Cn + Cn z + A1 Cn z + Cr z + a Cr z + a A1 Cr z)
A1=(wt1*tau/2)*(z+1)/(z-1);
A2=(wt2*tau/2)*(z+1)/(z-1);
olpideal
X1=ExpandAll[olpideal];
Y1=Together[X1];
Y2=ExpandDenominator[Y1]
ena1=Collect[Numerator[Y2],va]
duo1=Collect[ena1,vb]
tria=Collect[Denominator[Y2],z]
olpreal=duo1/tria
(vb*(Cn*tau^2*wt1*wt2 + Cn*tau^2*wt1*wt2*z -
       Cr*tau^2*wt1*wt2*z - a*Cr*tau^2*wt1*wt2*z -
       Cn*tau^2*wt1*wt2*z^2 - 2*Cr*tau^2*wt1*wt2*z^2 -
       2*a*Cr*tau^2*wt1*wt2*z^2 - Cn*tau^2*wt1*wt2*z^3 -
       Cr*tau^2*wt1*wt2*z^3 - a*Cr*tau^2*wt1*wt2*z^3) +
    va*(2*Cn*tau*wt2 - Cn*tau^2*wt1*wt2 - 2*Cn*tau*wt2*z -
       2*Cr*tau*wt2*z - 2*a*Cr*tau*wt2*z -
       Cn*tau^2*wt1*wt2*z + Cr*tau^2*wt1*wt2*z +
       a*Cr*tau^2*wt1*wt2*z - 2*Cn*tau*wt2*z^2 +
       Cn*tau^2*wt1*wt2*z^2 + 2*Cr*tau^2*wt1*wt2*z^2 +
       2*a*Cr*tau^2*wt1*wt2*z^2 + 2*Cn*tau*wt2*z^3 +
       2*Cr*tau*wt2*z^3 + 2*a*Cr*tau*wt2*z^3 +
       Cn*tau^2*wt1*wt2*z^3 + Cr*tau^2*wt1*wt2*z^3 +
       a*Cr*tau^2*wt1*wt2*z^3))/
  (-4*Cn + 2*Cn*tau*wt1 +
  (12*Cn + 4*Cr + 4*a*Cr - 2*Cn*tau*wt1 - 2*a*Cr*tau*wt1)*z +
  (-12*Cn - 8*Cr - 8*a*Cr - 2*Cn*tau*wt1)*z^2 +
  (4*Cn + 4*Cr + 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1)*z^3)
Aplus=(2*Cn*tau*wt2 - Cn*tau^2*wt1*wt2 - 2*Cn*tau*wt2*z -
       2*Cr*tau*wt2*z - 2*a*Cr*tau*wt2*z -
       Cn*tau^2*wt1*wt2*z + Cr*tau^2*wt1*wt2*z +
       a*Cr*tau^2*wt1*wt2*z - 2*Cn*tau*wt2*z^2 +
       Cn*tau^2*wt1*wt2*z^2 + 2*Cr*tau^2*wt1*wt2*z^2 +
       2*a*Cr*tau^2*wt1*wt2*z^2 + 2*Cn*tau*wt2*z^3 +
       2*Cr*tau*wt2*z^3 + 2*a*Cr*tau*wt2*z^3 +
       Cn*tau^2*wt1*wt2*z^3 + Cr*tau^2*wt1*wt2*z^3 +
       a*Cr*tau^2*wt1*wt2*z^3)/
```

```
    (-4*Cn + 2*Cn*tau*wt1 +
    (12*Cn + 4*Cr + 4*a*Cr - 2*Cn*tau*wt1 - 2*a*Cr*tau*wt1)*z +
    (-12*Cn - 8*Cr - 8*a*Cr - 2*Cn*tau*wt1)*z^2 +
    (4*Cn + 4*Cr + 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1)*z^3)

Aminus=-(Cn*tau^2*wt1*wt2 + Cn*tau^2*wt1*wt2*z -
        Cr*tau^2*wt1*wt2*z - a*Cr*tau^2*wt1*wt2*z -
        Cn*tau^2*wt1*wt2*z^2 - 2*Cr*tau^2*wt1*wt2*z^2 -
        2*a*Cr*tau^2*wt1*wt2*z^2 - Cn*tau^2*wt1*wt2*z^3 -
        Cr*tau^2*wt1*wt2*z^3 - a*Cr*tau^2*wt1*wt2*z^3) /
    (-4*Cn + 2*Cn*tau*wt1 +
    (12*Cn + 4*Cr + 4*a*Cr - 2*Cn*tau*wt1 - 2*a*Cr*tau*wt1)*z +
    (-12*Cn - 8*Cr - 8*a*Cr - 2*Cn*tau*wt1)*z^2 +
    (4*Cn + 4*Cr + 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1)*z^3)
```

```
C2OA1 : MOFR, The buffer transfer function


tbuf=Aplus/(1+Aminus)
tbf1=ExpandAll[tbuf];
tbf2=Together[tbf1];
tbf3=Collect[Numerator[tbf2],z];
tbf4=Collect[Denominator[tbf2],z];
tbuffer=tbf3/tbf4
(2*Cn*tau*wt2 - Cn*tau^2*wt1*wt2 +
(-2*Cn*tau*wt2 - 2*Cr*tau*wt2 - 2*a*Cr*tau*wt2 -
Cn*tau^2*wt1*wt2 + Cr*tau^2*wt1*wt2 +
a*Cr*tau^2*wt1*wt2)*z +
(-2*Cn*tau*wt2 + Cn*tau^2*wt1*wt2 +
2*Cr*tau^2*wt1*wt2 + 2*a*Cr*tau^2*wt1*wt2)*z^2 +
(2*Cn*tau*wt2 + 2*Cr*tau*wt2 + 2*a*Cr*tau*wt2 +
Cn*tau^2*wt1*wt2 + Cr*tau^2*wt1*wt2 +
a*Cr*tau^2*wt1*wt2)*z^3)/
(-4*Cn + 2*Cn*tau*wt1 - Cn*tau^2*wt1*wt2 +
(12*Cn + 4*Cr + 4*a*Cr - 2*Cn*tau*wt1 -
2*a*Cr*tau*wt1 - Cn*tau^2*wt1*wt2 +
Cr*tau^2*wt1*wt2 + a*Cr*tau^2*wt1*wt2)*z +
(-12*Cn - 8*Cr - 8*a*Cr - 2*Cn*tau*wt1 +
Cn*tau^2*wt1*wt2 + 2*Cr*tau^2*wt1*wt2 +
2*a*Cr*tau^2*wt1*wt2)*z^2 +
(4*Cn + 4*Cr + 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1 +
Cn*tau^2*wt1*wt2 + Cr*tau^2*wt1*wt2 +
a*Cr*tau^2*wt1*wt2)*z^3)

wt1=6.5285*10^6;
wt2=6.5285*10^6;
Cr=1*10^(-12);
Cn=6*10^(-12);
a=1;
tau=1*10^(-6);
tbuffer
                -10                -10                  -10  2
(-1.77386 10    - 2.74941 10    z + 3.47871 10    z  +

                -10  3
   4.45426 10    z ) /

                -10                -10                  -10  2
 (-2.01386 10    - 1.81884 10    z + 2.59871 10    z  +

                -10  3
   4.64369 10    z )
ARIT=Numerator[tbuffer]/(4.64369*10^(-10)*z^3)
```

```
ARIT1=Expand[ARIT]
PAR=Denominator[tbuffer]/(4.64369*10^(-10)*z^3)
PAR1=Expand[PAR]
transfer=ARIT1/PAR1
```

$$\frac{0.959208 - \frac{0.381993}{z^3} - \frac{0.592075}{z^2} + \frac{0.749126}{z}}{1. - \frac{0.433676}{z^3} - \frac{0.39168}{z^2} + \frac{0.559622}{z}}$$

General solution to an inverting configuration operational amplifier

```
Solve[{(v1-v2)/R1-(v2-v3)/R2==0,
        v3+(v2*Aminus)==0},{v1,v2}]
{{v1 -> -((R1*v3)/R2) + ((-R1 - R2)*v3)/(Aminus*R2),
   v2 -> -(v3/Aminus)}}
v1=-((R1*v3)/R2) + ((-R1 - R2)*v3)/(Aminus*R2)
  R1 v3     (-R1 - R2) v3
-(-----) + ---------------
   R2          Aminus R2
vinp=Collect[v1,v3]
   R1     -R1 - R2
(-(--) + ---------) v3
   R2     Aminus R2
invt=vinp/v3
  R1     -R1 - R2
-(--) + ---------
  R2     Aminus R2
invtr=ExpandAll[invt];
invtra=Together[invtr]
-R1 - Aminus R1 - R2
--------------------
     Aminus R2
tra=1/invtra
     Aminus R2
--------------------
-R1 - Aminus R1 - R2
```

```
C2OA1 : MOFR inverting circuit solution with capacitor
ratio=1 and gain=-1


trns=(Aminus*R2)/(-R1-R2-Aminus*R1)

Aminus=-(Cn*tau^2*wt1*wt2 + Cn*tau^2*wt1*wt2*z -
    Cr*tau^2*wt1*wt2*z - a*Cr*tau^2*wt1*wt2*z -
    Cn*tau^2*wt1*wt2*z^2 - 2*Cr*tau^2*wt1*wt2*z^2 -
    2*a*Cr*tau^2*wt1*wt2*z^2 - Cn*tau^2*wt1*wt2*z^3 -
    Cr*tau^2*wt1*wt2*z^3 - a*Cr*tau^2*wt1*wt2*z^3)/
 (-4*Cn + 2*Cn*tau*wt1 +
  (12*Cn + 4*Cr + 4*a*Cr - 2*Cn*tau*wt1 - 2*a*Cr*tau*wt1)*z +
  (-12*Cn - 8*Cr - 8*a*Cr - 2*Cn*tau*wt1)*z^2 +
  (4*Cn + 4*Cr + 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1)*z^3)
trns

X=ExpandAll[trns];

Y=Together[X];

NM=Collect[Numerator[Y],z]

DN=Collect[Denominator[Y],z]

invgainmofr=NM/DN

(Cn*R2*tau^2*wt1*wt2 + (Cn*R2*tau^2*wt1*wt2 -
Cr*R2*tau^2*wt1*wt2 - a*Cr*R2*tau^2*wt1*wt2)*z +
(-(Cn*R2*tau^2*wt1*wt2) - 2*Cr*R2*tau^2*wt1*wt2 -
2*a*Cr*R2*tau^2*wt1*wt2)*z^2 +
(-(Cn*R2*tau^2*wt1*wt2) - Cr*R2*tau^2*wt1*wt2 -
a*Cr*R2*tau^2*wt1*wt2)*z^3)/
(-4*Cn*R1 - 4*Cn*R2 + 2*Cn*R1*tau*wt1 + 2*Cn*R2*tau*wt1 -
Cn*R1*tau^2*wt1*wt2 + (12*Cn*R1 + 4*Cr*R1 + 4*a*Cr*R1 +
12*Cn*R2 + 4*Cr*R2 + 4*a*Cr*R2 - 2*Cn*R1*tau*wt1 -
2*a*Cr*R1*tau*wt1 - 2*Cn*R2*tau*wt1 - 2*a*Cr*R2*tau*wt1 -
Cn*R1*tau^2*wt1*wt2 + Cr*R1*tau^2*wt1*wt2 +
a*Cr*R1*tau^2*wt1*wt2)*z +
(-12*Cn*R1 - 8*Cr*R1 - 8*a*Cr*R1 - 12*Cn*R2 - 8*Cr*R2 -
8*a*Cr*R2 - 2*Cn*R1*tau*wt1 - 2*Cn*R2*tau*wt1 +
Cn*R1*tau^2*wt1*wt2 + 2*Cr*R1*tau^2*wt1*wt2 +
2*a*Cr*R1*tau^2*wt1*wt2)*z^2 +
(4*Cn*R1 + 4*Cr*R1 + 4*a*Cr*R1 + 4*Cn*R2 + 4*Cr*R2 +
4*a*Cr*R2 + 2*Cn*R1*tau*wt1 + 2*a*Cr*R1*tau*wt1 +
2*Cn*R2*tau*wt1 + 2*a*Cr*R2*tau*wt1 +
Cn*R1*tau^2*wt1*wt2 + Cr*R1*tau^2*wt1*wt2 +
a*Cr*R1*tau^2*wt1*wt2)*z^3)

wt1=6.5285*10^6;
wt2=6.5285*10^6;
Cr=1*10^(-12);
Cn=6*10^(-12);
a=1;
tau=1*10^(-6);
R1=5000;
R2=5000;
```

```
invgainmofr
```

$$\frac{\left(1.27864\times10^{-6} + 8.52426\times10^{-7}\,z - 2.13107\times10^{-6}\,z^2 - 1.70485\times10^{-6}\,z^3\right)}{\left(-7.35219\times10^{-7} - 9.66416\times10^{-7}\,z + 4.67646\times10^{-7}\,z^2 + 2.93884\times10^{-6}\,z^3\right)}$$

```
ARIT=Numerator[invgainmofr]/(2.93884*10^(-6)*z^3);
ARIT1=Expand[ARIT]
PAR=Denominator[invgainmofr]/(2.93884*10^(-6)*z^3);
PAR1=Expand[PAR];
transfer=ARIT1/PAR1
```

$$\frac{-0.580111 + \frac{0.435083}{z^3} + \frac{0.290055}{z^2} - \frac{0.725138}{z}}{1. - \frac{0.250173}{z^3} - \frac{0.328843}{z^2} + \frac{0.159126}{z}}$$

```
C2OA1 : MOFR inverting circuit solution with capacitor
ratio=1 and gain=-100



trns=(Aminus*R2)/(-R1-R2-Aminus*R1)

Aminus=-(Cn*tau^2*wt1*wt2 + Cn*tau^2*wt1*wt2*z -
    Cr*tau^2*wt1*wt2*z - a*Cr*tau^2*wt1*wt2*z -
    Cn*tau^2*wt1*wt2*z^2 - 2*Cr*tau^2*wt1*wt2*z^2 -
    2*a*Cr*tau^2*wt1*wt2*z^2 - Cn*tau^2*wt1*wt2*z^3 -
    Cr*tau^2*wt1*wt2*z^3 - a*Cr*tau^2*wt1*wt2*z^3)/
 (-4*Cn + 2*Cn*tau*wt1 +
  (12*Cn + 4*Cr + 4*a*Cr - 2*Cn*tau*wt1 - 2*a*Cr*tau*wt1)*z +
  (-12*Cn - 8*Cr - 8*a*Cr - 2*Cn*tau*wt1)*z^2 +
  (4*Cn + 4*Cr + 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1)*z^3)
trns

X=ExpandAll[trns];

Y=Together[X];

NM=Collect[Numerator[Y],z]

DN=Collect[Denominator[Y],z]

invgainmofr=NM/DN
(Cn*R2*tau^2*wt1*wt2 + (Cn*R2*tau^2*wt1*wt2 -
Cr*R2*tau^2*wt1*wt2 - a*Cr*R2*tau^2*wt1*wt2)*z +
(-(Cn*R2*tau^2*wt1*wt2) - 2*Cr*R2*tau^2*wt1*wt2 -
2*a*Cr*R2*tau^2*wt1*wt2)*z^2 +
(-(Cn*R2*tau^2*wt1*wt2) - Cr*R2*tau^2*wt1*wt2 -
a*Cr*R2*tau^2*wt1*wt2)*z^3)/
(-4*Cn*R1 - 4*Cn*R2 + 2*Cn*R1*tau*wt1 + 2*Cn*R2*tau*wt1 -
Cn*R1*tau^2*wt1*wt2 +
(12*Cn*R1 + 4*Cr*R1 + 4*a*Cr*R1 + 12*Cn*R2 + 4*Cr*R2 +
4*a*Cr*R2 - 2*Cn*R1*tau*wt1 - 2*a*Cr*R1*tau*wt1 -
2*Cn*R2*tau*wt1 - 2*a*Cr*R2*tau*wt1 -
Cn*R1*tau^2*wt1*wt2 + Cr*R1*tau^2*wt1*wt2 +
a*Cr*R1*tau^2*wt1*wt2)*z +
(-12*Cn*R1 - 8*Cr*R1 - 8*a*Cr*R1 - 12*Cn*R2 - 8*Cr*R2 -
8*a*Cr*R2 - 2*Cn*R1*tau*wt1 - 2*Cn*R2*tau*wt1 +
Cn*R1*tau^2*wt1*wt2 + 2*Cr*R1*tau^2*wt1*wt2 +
2*a*Cr*R1*tau^2*wt1*wt2)*z^2 +
(4*Cn*R1 + 4*Cr*R1 + 4*a*Cr*R1 + 4*Cn*R2 + 4*Cr*R2 +
4*a*Cr*R2 + 2*Cn*R1*tau*wt1 + 2*a*Cr*R1*tau*wt1 +
2*Cn*R2*tau*wt1 + 2*a*Cr*R2*tau*wt1 +
Cn*R1*tau^2*wt1*wt2 + Cr*R1*tau^2*wt1*wt2 +
a*Cr*R1*tau^2*wt1*wt2)*z^3)

wt1=6.5285*10^6;
wt2=6.5285*10^6;
Cr=1*10^(-12);
Cn=6*10^(-12);
a=1;
tau=1*10^(-6);
R1=500;
R2=50000;
```

```
invgainmofr
```

$$(0.0000127864 + 8.52426\ 10^{-6}\ z - 0.0000213107\ z^2 - 0.0000170485\ z^3)\ /$$

$$(2.61641\ 10^{-6} - 6.60892\ 10^{-7}\ z - 8.18716\ 10^{-6}\ z^2 + 6.40213\ 10^{-6}\ z^3)$$

```
ARIT=Numerator[invgainmofr]/(6.40213*10^(-6)*z^3);
ARIT1=Expand[ARIT];
PAR=Denominator[invgainmofr]/(6.40213*10^(-6)*z^3);
PAR1=Expand[PAR];
transfer=ARIT1/PAR1
```

$$\frac{-2.66295 + \frac{1.99721}{z^3} + \frac{1.33147}{z^2} - \frac{3.32868}{z}}{1. + \frac{0.408678}{z^3} - \frac{0.10323}{z^2} - \frac{1.27882}{z}}$$

```
C2OA1 : MOFR inverting circuit solution with capacitor
ratio=8 and gain=-100


trns=(Aminus*R2)/(-R1-R2-Aminus*R1)

Aminus=-(Cn*tau^2*wt1*wt2 + Cn*tau^2*wt1*wt2*z -
    Cr*tau^2*wt1*wt2*z - a*Cr*tau^2*wt1*wt2*z -
    Cn*tau^2*wt1*wt2*z^2 - 2*Cr*tau^2*wt1*wt2*z^2 -
    2*a*Cr*tau^2*wt1*wt2*z^2 - Cn*tau^2*wt1*wt2*z^3 -
    Cr*tau^2*wt1*wt2*z^3 - a*Cr*tau^2*wt1*wt2*z^3)/
 (-4*Cn + 2*Cn*tau*wt1 +
  (12*Cn + 4*Cr + 4*a*Cr - 2*Cn*tau*wt1 - 2*a*Cr*tau*wt1)*z +
  (-12*Cn - 8*Cr - 8*a*Cr - 2*Cn*tau*wt1)*z^2 +
  (4*Cn + 4*Cr + 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1)*z^3)
trns

X=ExpandAll[trns];

Y=Together[X];

NM=Collect[Numerator[Y],z]

DN=Collect[Denominator[Y],z]

invgainmofr=NM/DN

(Cn*R2*tau^2*wt1*wt2 +
(Cn*R2*tau^2*wt1*wt2 - Cr*R2*tau^2*wt1*wt2 -
a*Cr*R2*tau^2*wt1*wt2)*z +
(-(Cn*R2*tau^2*wt1*wt2) - 2*Cr*R2*tau^2*wt1*wt2 -
2*a*Cr*R2*tau^2*wt1*wt2)*z^2 +
(-(Cn*R2*tau^2*wt1*wt2) - Cr*R2*tau^2*wt1*wt2 -
a*Cr*R2*tau^2*wt1*wt2)*z^3)/
(-4*Cn*R1 - 4*Cn*R2 + 2*Cn*R1*tau*wt1 +
2*Cn*R2*tau*wt1 - Cn*R1*tau^2*wt1*wt2 +
(12*Cn*R1 + 4*Cr*R1 + 4*a*Cr*R1 + 12*Cn*R2 +
4*Cr*R2 + 4*a*Cr*R2 - 2*Cn*R1*tau*wt1 -
2*a*Cr*R1*tau*wt1 - 2*Cn*R2*tau*wt1 -
2*a*Cr*R2*tau*wt1 - Cn*R1*tau^2*wt1*wt2 +
Cr*R1*tau^2*wt1*wt2 + a*Cr*R1*tau^2*wt1*wt2)*z +
(-12*Cn*R1 - 8*Cr*R1 - 8*a*Cr*R1 - 12*Cn*R2 -
8*Cr*R2 - 8*a*Cr*R2 - 2*Cn*R1*tau*wt1 -
2*Cn*R2*tau*wt1 + Cn*R1*tau^2*wt1*wt2 +
2*Cr*R1*tau^2*wt1*wt2 + 2*a*Cr*R1*tau^2*wt1*wt2)*
z^2 + (4*Cn*R1 + 4*Cr*R1 + 4*a*Cr*R1 + 4*Cn*R2 +
4*Cr*R2 + 4*a*Cr*R2 + 2*Cn*R1*tau*wt1 +
2*a*Cr*R1*tau*wt1 + 2*Cn*R2*tau*wt1 +
2*a*Cr*R2*tau*wt1 + Cn*R1*tau^2*wt1*wt2 +
Cr*R1*tau^2*wt1*wt2 + a*Cr*R1*tau^2*wt1*wt2)*z^3)

wt1=6.5285*10^6;
wt2=6.5285*10^6;
Cr=1*10^(-12);
Cn=6*10^(-12);
a=8;
tau=1*10^(-6);
R1=500;
```

```
R2=50000;
invgainmofr
(0.000012786393675 - 6.393196837500004*10^-6*z -
0.000051145574700000002*z^2 -
0.000031965984187500001*z^3)/
(2.61640706325*10^-6 - 3.713367031625002*10^-6*z -
0.000010716815253*z^2 + 0.000012580958841875*z^3)
ARIT=Numerator[invgainmofr]/(0.000012580958841875*z^3);
ARIT1=Expand[ARIT];
PAR=Denominator[invgainmofr]/(0.000012580958841875*z^3);
PAR1=Expand[PAR];
transfer=ARIT1/PAR1
```

$$\frac{-2.54082 + \frac{1.01633}{z^3} - \frac{0.508165}{z^2} - \frac{4.06532}{z}}{1. + \frac{0.207966}{z^3} - \frac{0.295158}{z^2} - \frac{0.851828}{z}}$$

```
C2OA1 : MOFR inverting circuit solution with capacitor
ratio=0.1 and gain=-100


invmofr=(Cn*R2*tau^2*wt1*wt2 + (Cn*R2*tau^2*wt1*wt2 -
 Cr*R2*tau^2*wt1*wt2 - a*Cr*R2*tau^2*wt1*wt2)*z +
 (-(Cn*R2*tau^2*wt1*wt2) - 2*Cr*R2*tau^2*wt1*wt2 -
 2*a*Cr*R2*tau^2*wt1*wt2)*z^2 +
 (-(Cn*R2*tau^2*wt1*wt2) - Cr*R2*tau^2*wt1*wt2 -
 a*Cr*R2*tau^2*wt1*wt2)*z^3)/
 (-4*Cn*R1 - 4*Cn*R2 + 2*Cn*R1*tau*wt1 + 2*Cn*R2*tau*wt1 -
 Cn*R1*tau^2*wt1*wt2 +
 (12*Cn*R1 + 4*Cr*R1 + 4*a*Cr*R1 + 12*Cn*R2 + 4*Cr*R2 +
 4*a*Cr*R2 - 2*Cn*R1*tau*wt1 - 2*a*Cr*R1*tau*wt1 -
 2*Cn*R2*tau*wt1 - 2*a*Cr*R2*tau*wt1 -
 Cn*R1*tau^2*wt1*wt2 + Cr*R1*tau^2*wt1*wt2 +
 a*Cr*R1*tau^2*wt1*wt2)*z +
 (-12*Cn*R1 - 8*Cr*R1 - 8*a*Cr*R1 - 12*Cn*R2 - 8*Cr*R2 -
 8*a*Cr*R2 - 2*Cn*R1*tau*wt1 - 2*Cn*R2*tau*wt1 +
 Cn*R1*tau^2*wt1*wt2 + 2*Cr*R1*tau^2*wt1*wt2 +
 2*a*Cr*R1*tau^2*wt1*wt2)*z^2 +
 (4*Cn*R1 + 4*Cr*R1 + 4*a*Cr*R1 + 4*Cn*R2 + 4*Cr*R2 +
 4*a*Cr*R2 + 2*Cn*R1*tau*wt1 + 2*a*Cr*R1*tau*wt1 +
 2*Cn*R2*tau*wt1 + 2*a*Cr*R2*tau*wt1 +
 Cn*R1*tau^2*wt1*wt2 + Cr*R1*tau^2*wt1*wt2 +
 a*Cr*R1*tau^2*wt1*wt2)*z^3);
wt1=6.5285*10^6;
wt2=6.5285*10^6;
Cr=1*10^(-12);
Cn=6*10^(-12);
a=0.1;
tau=1*10^(-6);
R1=500;
R2=50000;
invmofr
                                                    2
(0.0000127864 + 0.0000104422 z - 0.0000174747 z   -

                  3
   0.0000151306 z ) /

            -6                -7                  -6  2
 (2.61641 10    - 2.68431 10    z - 7.86192 10    z  +

             -6  3
   5.60771 10    z )
ARIT=Numerator[invmofr]/(5.60771*10^(-6)*z^3);
ARIT1=Expand[ARIT];
PAR=Denominator[invmofr]/(5.60771*10^(-6)*z^3);
PAR1=Expand[PAR];
```

transfer=ARIT1/PAR1

$$\frac{-2.69817 + \frac{2.28015}{z^3} + \frac{1.86212}{z^2} - \frac{3.1162}{z}}{1. + \frac{0.466573}{z^3} - \frac{0.0478682}{z^2} - \frac{1.40198}{z}}$$

```
C2OA1 : TSI, Real open loop and buffer
transfer function


Solve[{vout==(va-v1)*A2,
 v1==(vb-v2)*A1,
 (va-v2)*(-Cr*z^-1)==(v2-v1)*(Cn(1-z^-1)-a*Cr*z^-1)},
 {v1,v2,vout}]
{{vout -> A2*va + A2*(-(A1*vb) -
        (A1*(-(Cr*va) + A1*vb*(-Cn - a*Cr + Cn*z)))/
         (Cn + Cr + a*Cr - Cn*z - A1*(-Cn - a*Cr + Cn*z))
        ), v1 ->
    A1*vb + (A1*(-(Cr*va) + A1*vb*(-Cn - a*Cr + Cn*z)))/
      (Cn + Cr + a*Cr - Cn*z - A1*(-Cn - a*Cr + Cn*z)),
   v2 -> -((-(Cr*va) + A1*vb*(-Cn - a*Cr + Cn*z))/
       (Cn + Cr + a*Cr - Cn*z - A1*(-Cn - a*Cr + Cn*z)))}}
vout=A2*va + A2*(-(A1*vb) -
     (A1*(-(Cr*va) + A1*vb*(-Cn - a*Cr + Cn*z)))/
     (Cn + Cr + a*Cr - Cn*z - A1*(-Cn - a*Cr + Cn*z)))

X=ExpandAll[vout];
Y=Together[X]
ena=Collect[Numerator[Y],va]
duo=Collect[ena,vb]
olpideal=duo/Denominator[Y]
(va*(A2*Cn + A1*A2*Cn + A2*Cr + a*A2*Cr + A1*A2*Cr +
a*A1*A2*Cr - A2*Cn*z - A1*A2*Cn*z) +
vb*(-(A1*A2*Cn) - A1*A2*Cr - a*A1*A2*Cr + A1*A2*Cn*z))
/(Cn + A1*Cn + Cr + a*Cr + a*A1*Cr - Cn*z - A1*Cn*z)

A1=(wt1*tau/2)*(z+1)/(z-1);
A2=(wt2*tau/2)*(z+1)/(z-1);
olpideal;
X1=ExpandAll[olpideal];
Y1=Together[X1]
Y2=ExpandDenominator[Y1]
ena1=Collect[Numerator[Y2],va];
duo1=Collect[ena1,vb];
tria=Collect[Denominator[Y2],z]
```

```
olprealtsi=duo1/tria;

(vb*(Cn*tau^2*wt1*wt2 + Cr*tau^2*wt1*wt2 +
a*Cr*tau^2*wt1*wt2 + Cn*tau^2*wt1*wt2*z +
2*Cr*tau^2*wt1*wt2*z + 2*a*Cr*tau^2*wt1*wt2*z -
Cn*tau^2*wt1*wt2*z^2 + Cr*tau^2*wt1*wt2*z^2 +
a*Cr*tau^2*wt1*wt2*z^2 - Cn*tau^2*wt1*wt2*z^3) +
va*(2*Cn*tau*wt2 + 2*Cr*tau*wt2 + 2*a*Cr*tau*wt2 -
Cn*tau^2*wt1*wt2 - Cr*tau^2*wt1*wt2 -
a*Cr*tau^2*wt1*wt2 - 2*Cn*tau*wt2*z -
Cn*tau^2*wt1*wt2*z - 2*Cr*tau^2*wt1*wt2*z -
2*a*Cr*tau^2*wt1*wt2*z - 2*Cn*tau*wt2*z^2 -
2*Cr*tau*wt2*z^2 - 2*a*Cr*tau*wt2*z^2 +
Cn*tau^2*wt1*wt2*z^2 - Cr*tau^2*wt1*wt2*z^2 -
a*Cr*tau^2*wt1*wt2*z^2 + 2*Cn*tau*wt2*z^3 +
Cn*tau^2*wt1*wt2*z^3))/
(-4*Cn - 4*Cr - 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1 +
(12*Cn + 8*Cr + 8*a*Cr - 2*Cn*tau*wt1)*z +
(-12*Cn - 4*Cr - 4*a*Cr - 2*Cn*tau*wt1 -
2*a*Cr*tau*wt1)*z^2 + (4*Cn + 2*Cn*tau*wt1)*z^3)

Aplus=(2*Cn*tau*wt2 + 2*Cr*tau*wt2 + 2*a*Cr*tau*wt2 -
 Cn*tau^2*wt1*wt2 - Cr*tau^2*wt1*wt2 -
 a*Cr*tau^2*wt1*wt2 - 2*Cn*tau*wt2*z -
 Cn*tau^2*wt1*wt2*z - 2*Cr*tau^2*wt1*wt2*z -
 2*a*Cr*tau^2*wt1*wt2*z - 2*Cn*tau*wt2*z^2 -
 2*Cr*tau*wt2*z^2 - 2*a*Cr*tau*wt2*z^2 +
 Cn*tau^2*wt1*wt2*z^2 - Cr*tau^2*wt1*wt2*z^2 -
 a*Cr*tau^2*wt1*wt2*z^2 + 2*Cn*tau*wt2*z^3 +
 Cn*tau^2*wt1*wt2*z^3)/
 (-4*Cn - 4*Cr - 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1+
 (12*Cn + 8*Cr + 8*a*Cr - 2*Cn*tau*wt1)*z +
 (-12*Cn - 4*Cr - 4*a*Cr - 2*Cn*tau*wt1 -
 2*a*Cr*tau*wt1)*z^2 + (4*Cn + 2*Cn*tau*wt1)*z^3);

Aminus=-(Cn*tau^2*wt1*wt2 + Cr*tau^2*wt1*wt2 +
 a*Cr*tau^2*wt1*wt2 + Cn*tau^2*wt1*wt2*z +
 2*Cr*tau^2*wt1*wt2*z + 2*a*Cr*tau^2*wt1*wt2*z -
 Cn*tau^2*wt1*wt2*z^2 + Cr*tau^2*wt1*wt2*z^2 +
 a*Cr*tau^2*wt1*wt2*z^2 - Cn*tau^2*wt1*wt2*z^3)/
 (-4*Cn - 4*Cr - 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1+
 (12*Cn + 8*Cr + 8*a*Cr - 2*Cn*tau*wt1)*z +
 (-12*Cn - 4*Cr - 4*a*Cr - 2*Cn*tau*wt1 -
 2*a*Cr*tau*wt1)*z^2 + (4*Cn + 2*Cn*tau*wt1)*z^3);

trns=Aplus/(1+Aminus)

X3=ExpandAll[trns];

Y3=Together[X3];

ena2=Collect[Numerator[Y3],z];

duo2=Collect[Denominator[Y3],z];
```

```
transfer=ena2/duo2
(2*Cn*tau*wt2 + 2*Cr*tau*wt2 + 2*a*Cr*tau*wt2 -
Cn*tau^2*wt1*wt2 - Cr*tau^2*wt1*wt2 -
a*Cr*tau^2*wt1*wt2 +
(-2*Cn*tau*wt2 - Cn*tau^2*wt1*wt2 -
2*Cr*tau^2*wt1*wt2 - 2*a*Cr*tau^2*wt1*wt2)*z +
(-2*Cn*tau*wt2 - 2*Cr*tau*wt2 - 2*a*Cr*tau*wt2 +
Cn*tau^2*wt1*wt2 - Cr*tau^2*wt1*wt2 -
a*Cr*tau^2*wt1*wt2)*z^2 +
(2*Cn*tau*wt2 + Cn*tau^2*wt1*wt2)*z^3)/
(-4*Cn - 4*Cr - 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1 -
Cn*tau^2*wt1*wt2 - Cr*tau^2*wt1*wt2 -
a*Cr*tau^2*wt1*wt2 +
(12*Cn + 8*Cr + 8*a*Cr - 2*Cn*tau*wt1 -
Cn*tau^2*wt1*wt2 - 2*Cr*tau^2*wt1*wt2 -
2*a*Cr*tau^2*wt1*wt2)*z +
(-12*Cn - 4*Cr - 4*a*Cr - 2*Cn*tau*wt1 -
2*a*Cr*tau*wt1 + Cn*tau^2*wt1*wt2 -
Cr*tau^2*wt1*wt2 - a*Cr*tau^2*wt1*wt2)*z^2 +
(4*Cn + 2*Cn*tau*wt1 + Cn*tau^2*wt1*wt2)*z^3)

wt1=6.5285*10^6;
wt2=6.5285*10^6;
Cr=1*10^(-12);
Cn=6*10^(-12);
a=1;
tau=1*10^(-6);
transfer
             -10               -10                  -11  2
(-2.36514 10    - 5.04555 10    z + 6.60292 10    z  +

             -10  3
   3.3407 10    z ) /

              -10               -10                  -13  2
 (-2.81571 10    - 4.16555 10    z - 9.13751 10    z  +

             -10  3
   3.5807 10    z )
ARIT=Numerator[transfer]/(3.5807*10^(-10)*z^3);
ARIT1=Expand[ARIT];
PAR=Denominator[transfer]/(3.5807*10^(-10)*z^3);
PAR1=Expand[PAR]
```

tbfnum=ARIT1/PAR1

$$\frac{0.932974 - \frac{0.660526}{z^3} - \frac{1.4091}{z^2} + \frac{0.184403}{z}}{1. - \frac{0.786359}{z^3} - \frac{1.16333}{z^2} - \frac{0.00255188}{z}}$$

```
C2OA1 : TSI, Real buffer transfer function
with Cr=0.05


Aplus=(2*Cn*tau*wt2 + 2*Cr*tau*wt2 + 2*a*Cr*tau*wt2 -
       Cn*tau^2*wt1*wt2 - Cr*tau^2*wt1*wt2 -
       a*Cr*tau^2*wt1*wt2 - 2*Cn*tau*wt2*z -
       Cn*tau^2*wt1*wt2*z - 2*Cr*tau^2*wt1*wt2*z -
       2*a*Cr*tau^2*wt1*wt2*z - 2*Cn*tau*wt2*z^2 -
       2*Cr*tau*wt2*z^2 - 2*a*Cr*tau*wt2*z^2 +
       Cn*tau^2*wt1*wt2*z^2 - Cr*tau^2*wt1*wt2*z^2 -
       a*Cr*tau^2*wt1*wt2*z^2 + 2*Cn*tau*wt2*z^3 +
       Cn*tau^2*wt1*wt2*z^3)/
  (-4*Cn - 4*Cr - 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1+
  (12*Cn + 8*Cr + 8*a*Cr - 2*Cn*tau*wt1)*z +
  (-12*Cn - 4*Cr - 4*a*Cr - 2*Cn*tau*wt1 -
  2*a*Cr*tau*wt1)*z^2 + (4*Cn + 2*Cn*tau*wt1)*z^3);

Aminus=-(Cn*tau^2*wt1*wt2 + Cr*tau^2*wt1*wt2 +
  a*Cr*tau^2*wt1*wt2 + Cn*tau^2*wt1*wt2*z +
  2*Cr*tau^2*wt1*wt2*z + 2*a*Cr*tau^2*wt1*wt2*z -
  Cn*tau^2*wt1*wt2*z^2 + Cr*tau^2*wt1*wt2*z^2 +
  a*Cr*tau^2*wt1*wt2*z^2 - Cn*tau^2*wt1*wt2*z^3)/
  (-4*Cn - 4*Cr - 4*a*Cr + 2*Cn*tau*wt1 + 2*a*Cr*tau*wt1 +
  (12*Cn + 8*Cr + 8*a*Cr - 2*Cn*tau*wt1)*z +
  (-12*Cn - 4*Cr - 4*a*Cr - 2*Cn*tau*wt1 -
  2*a*Cr*tau*wt1)*z^2 + (4*Cn + 2*Cn*tau*wt1)*z^3);

trns=Aplus/(1+Aminus);

X3=ExpandAll[trns];

Y3=Together[X3];

ena2=Collect[Numerator[Y3],z];

duo2=Collect[Denominator[Y3],z];

transfer=ena2/duo2;

wt1=6.5285*10^6;
wt2=6.5285*10^6;
Cr=0.05*10^(-12);
Cn=6*10^(-12);
a=1;
tau=1*10^(-6);
```

```
transfer
```

$$\frac{(-1.80342\times10^{-10} - 3.42594\times10^{-10}\,z + 1.71818\times10^{-10}\,z^2 + 3.3407\times10^{-10}\,z^3)}{(-2.05395\times10^{-10} - 2.69794\times10^{-10}\,z + 1.00071\times10^{-10}\,z^2 + 3.5807\times10^{-10}\,z^3)}$$

```
ARIT=Numerator[transfer]/(3.5807*10^(-10)*z^3);
ARIT1=Expand[ARIT];
PAR=Denominator[transfer]/(3.5807*10^(-10)*z^3);
PAR1=Expand[PAR];
tbfnum=ARIT1/PAR1
```

$$\frac{0.932974 - \frac{0.503651}{z^3} - \frac{0.95678}{z^2} + \frac{0.479845}{z}}{1. - \frac{0.573617}{z^3} - \frac{0.753468}{z^2} + \frac{0.279473}{z}}$$

APPENDIX B

ANALOG - DIGITAL MICROCHIP FABRICATION PARAMETERS

FTPed to ece.nps.navy.mil on 12/13/93.

ORBIT ELECTRICAL PARAMETERS

2UM, DOUBLE METAL, DOUBLE POLY, N-WELL CMOS
POLY 1 AND POLY 2 ACTIVE GATES
POLY 1 / 2 CAPACITORS
DEPLETION IMPLANT ADJUST FOR BURIED
CHANNEL POTENTIAL

A.1 Oxide Thicknesses (Angstroms)

		MIN	TYP	MAX
A.1.1	Poly 1 gate oxide	370	400	430
A.1.2	Poly 2 gate oxide	470	500	530
A.1.3	Field oxide (Poly 1 & 2 to Sub)	5500	6000	6500
A.1.4	Metal 1 to Poly 1 & 2	8000	8500	9000
A.1.5	Metal 1 to Sub	13500	14500	15500
A.1.6	Metal 1 to N+/P+ Diff	8500	9000	9500
A.1.7	Metal 2 to Metal 1	6000	6500	7000
A.1.8	Poly 1 to Poly 2	650	750	850

A.2 Conductors

A.2.1	Poly 1	3700	4000	4300
A.2.2	Poly 2	3700	4000	4300

A.2.3	Metal 1	5500 6000 6500
A.2.4	Metal 1	10500 11500 12500

B. TRANSISTOR SPECIFICATIONS

B.1 P Channel Poly 1

B.1.1	Threshold (volts)	-1.0 -0.75 -0.5
B.1.2	Gamma (volts **.)	.45 .55 .65
B.1.3	K'=uCox/2 (uA/v**2) (Vds=0.1V, Vgs=2-3V)	6.0 7.5 8.5
B.1.4	Punchthrough for min. length channel (volts)	-16 -14 -10
B.1.5	Subthreshold slope (volts**-3/decade)	90 100 110
B.1.6	Delta width = effective-mask (microns)	
B.1.7	Delta length = effective-mask (microns)	-0.7 -0.4 -0.1

B.2 P Channel Poly 2

B.2.1	Threshold (volts)	-1.5 -1.15 -0.8
B.2.2	Gamma (volts**.5	0.5 0.6 0.8
B.2.3	K'=uCox/2 (uA/v**2)	5.0 6.0 7
B.2.4	Punchthrough for min. length channel (volts)	-16 -14 -10
B.2.5	Subthreshold slope (volts**-3/decade)	
B.2.6	Delta width = effective-mask (microns)	
B.2.7	Delta length = effective-mask (microns)	-0.8 -0.5 -0.2

B.3 N Channel Poly 1

B.3.1	Threshold (volts)	0.5 0.75 1.0
B.3.2	Gamma (volts**.5)	.15 .25 .35
B.3.3	K'=ucox/2 (uA/v**2) (Vds=0.1V, Vgs=2-3V)	20 23 26
B.3.4	Subthreshold slope (volts**-3/decade)	90 100 110
B.3.5	Punchthrough for min. length channel (volts)	10 14 16
B.3.6	Delta width = effective-mask (microns)	
B.3.7	Delta length = effective-mask (microns)	-0.7 -0.3 0

B.4 N Channel Poly 2

B.4.1	Threshold (volts)	0.7 1.1 1.4
B.4.2	Gamma (volts**.5)	0.21 0.3 0.4
B.4.3	K'=uCox/2 (uA/v**2)	18 20 22
B.4.4	Subthreshold slope (volts**-3/decade)	
B.4.5	Punchthrough for min. length channel (volts)	10 14 16

B.4.6	Delta width = effective-drawn (microns)			
B.4.7	Delta length = effective-drawn (microns)	-0.8	-0.4	-0.1

B.5 CCD Channel Potential (volts)

B.5.1	Poly 1VG=0	3.0	5.0	8.0
B.5.2	Poly 2VG=0	3.0	5.0	8.0

B.6 NPN Transistor in the N-well

B.6.1 Beta= 80 to 200 at IB = 1 uA

B.6.2 BVEBO= 10 V
B.6.3 BVCEO> -10 V
B.6.4 BVCES> 10 V
B.6.5 BVCBO> -60 V

B.6.6 P-base Xj0.45 to 0.50 micron
B.6.7 N+emitter Xj0.3 micron

B.6.8 Rcollector1.0 +/- 0.2 Kohm/sq
B.6.9 P-base resistance1.2 +/- 0.2 Kohm/sq

B.6.10 Early Voltage> 30 V

C. SHEET RESISTANCES (OHMS PER SQUARE)

		MIN	TYP	MAX
		---	---	---
C.1	P+ Active		40 57	80
C.2	N+ Active		20 28	40
C.3	N Well (with field implant)	2000	2500	3000
C.4.1	Poly1		15 21	30
C.4.2	Poly2		18 25	30

C.5	Metal1	.050	.070	.090
C.6	Metal2	.030	.040	.050

D. CONTACT RESISTANCE (OHMS)

D.1	Metal1 to P+ Active	35	75
D.2	Metal1 to N+ Active	20	50
D.3.1	Metal1 to Poly1	20	50
D.3.2	Metal1 to Poly2	20	50
D.4	Metal1 to Metal2	0.4	0.7

(single contact 2 by 2um)

E. FIELD INVERSION AND BREAKDOWN VOLTAGES (VOLTS)

E.1.1	N Channel Poly1 field inversion	10	14
E.1.2	N Channel Poly2 field inversion	10	14
E.2	N Channel Metal1 field inversion	10	14
E.3	N Channel Metal2 field inversion		
E.4.1	Channel Poly1 field inversion	-14	-10
E.4.2	P Channel Poly2 field inversion	-14	-10
E.5	P Channel Metal1 field inversion	-14	-10
E.6	P Channel Metal2 field inversion		
E.7.1	N Diffusion to substrate junction breakdown	14	16
E.7.2	P Diffusion to substrate junction breakdown	15	18
E.8	N-well to P- sub junction breakdown	50	90

INTERLAYER CAPACITANCES

(PLATE: 10 ** -5 PF / MICRON ** 2 FRINGE: 10 ** -5 PF / MICRON)

	Capacitance		Equiv. Thickness	
	MIN	MAX	MIN	MAX
GATE OXIDE PLATE POLY1	78	90	370 Ang	430 Ang
GATE OXIDE PLATE POLY2	64	70	470 Ang	530 Ang
FIELD POLY1 TO SUBS FRINGE				
FIELD POLY2 TO SUBS FRINGE				
POLY1 TO POLY2 OVER ACTIVE	43	55	650 Ang	850 Ang
POLY1 TO POLY2 OVER FIELD	43	55	650 Ang	850 Ang
METAL1 TO ACTIVE PLATE	3.6	4.0	8500 Ang	9500 Ang
METAL1 TO ACTIVE FRINGE				
METAL1 TO SUBS PLATE	2.2	2.5	13500 Ang	15500 Ang
METAL1 TO POLY PLATE	3.7	4.4	8000 Ang	9000 Ang
METAL1 TO POLY FRINGE				
METAL2 TO ACTIVE PLATE	1.9	2.4	14500 Ang	17500 Ang
METAL2 TO ACTIVE FRINGE				
METAL2 TO SUBS PLATE	1.5	1.65	19500 Ang	22000 Ang
METAL2 TO SUBS FRINGE				
METAL2 TO POLY PLATE	1.9	2.4	14500 Ang	17500 Ang
METAL2 TO POLY FRINGE				
METAL2 TO METAL1 PLATE	4.6	5.6	6000 Ang	7500 Ang
METAL2 TO METAL1 FRINGE				

APPENDIX C

MAGIC CELL LAYOUTS

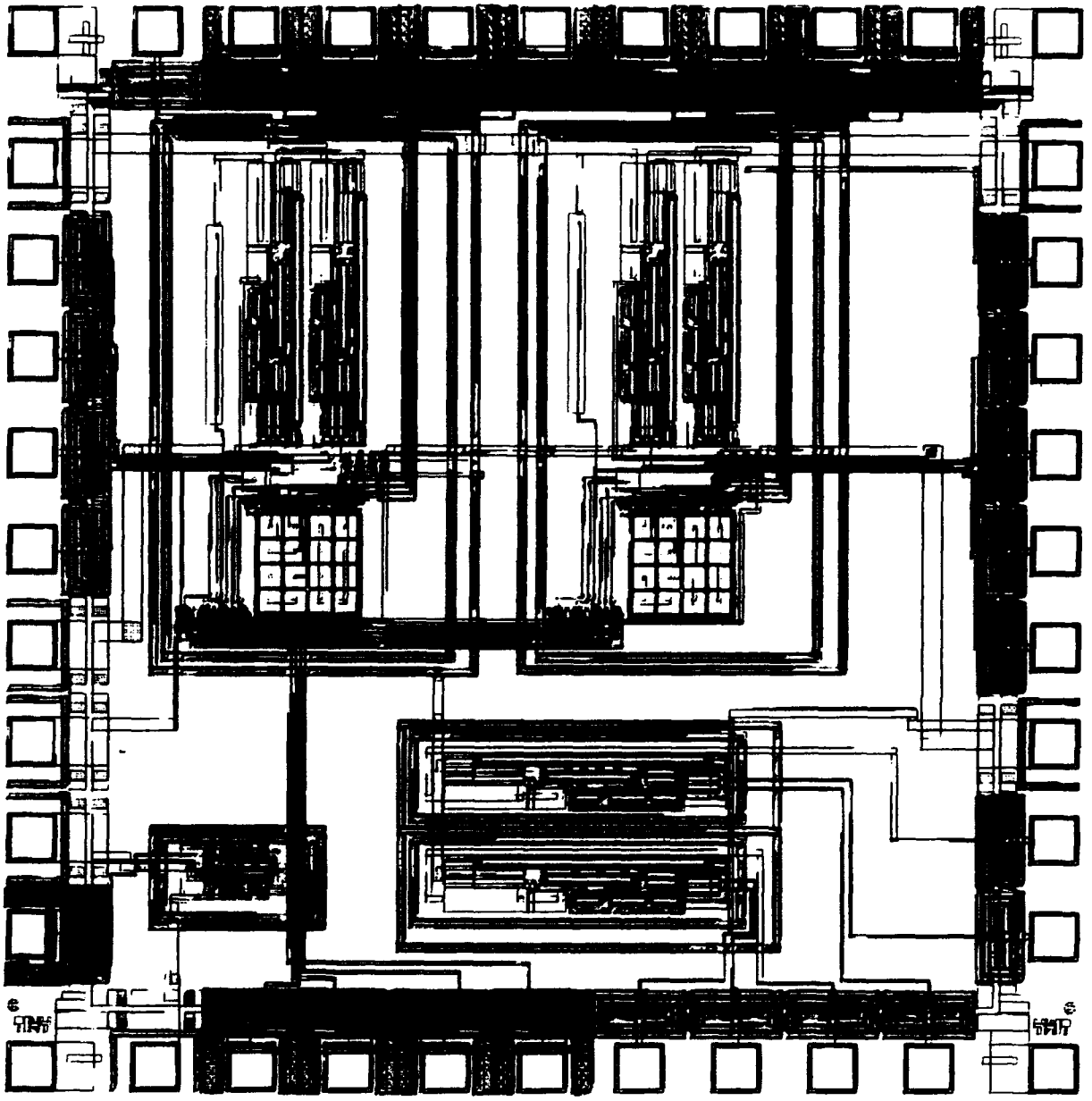


Figure ApC 1 Complete Microchip Layout Geometry As Submitted For Fabrication

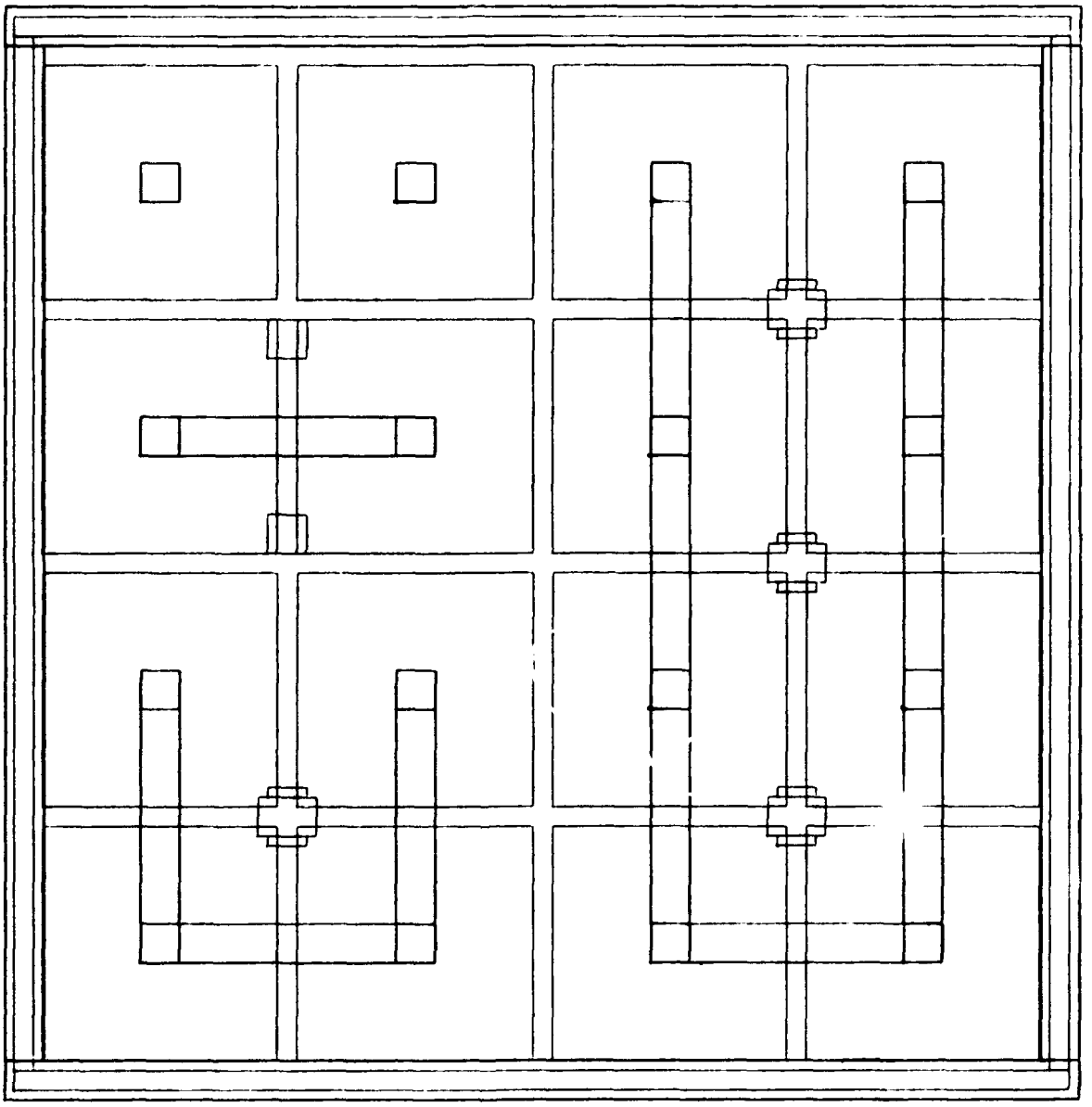


Figure ApC 2 Layout Geometry Of The Programmable Capacitor Ratio

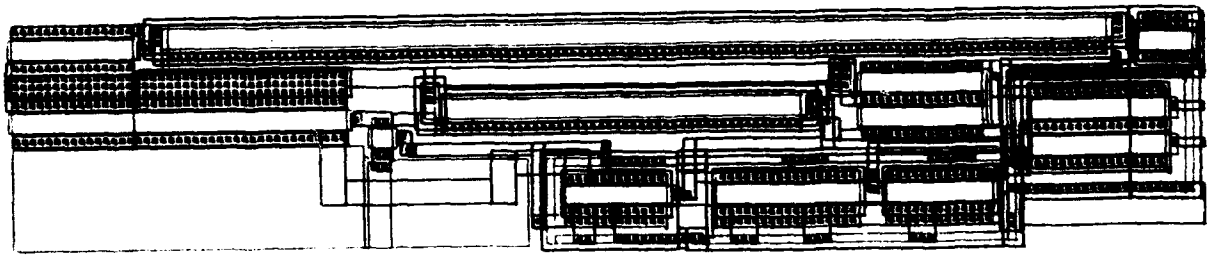


Figure ApC 3 CMOS Operational Amplifier Used As The Main Building Block In The Implementation Of The Composite C2OA - 1

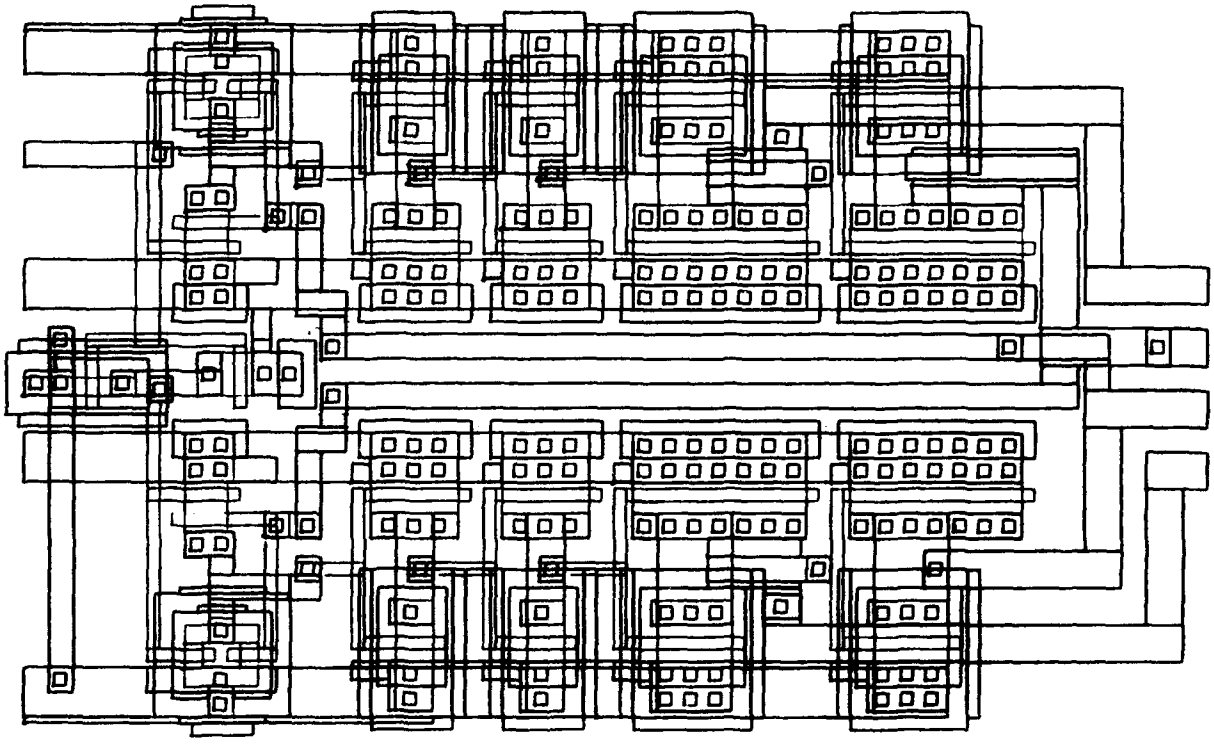


Figure ApC 4 Layout Geometry Of The Two Phase Non-Overlapping Clock

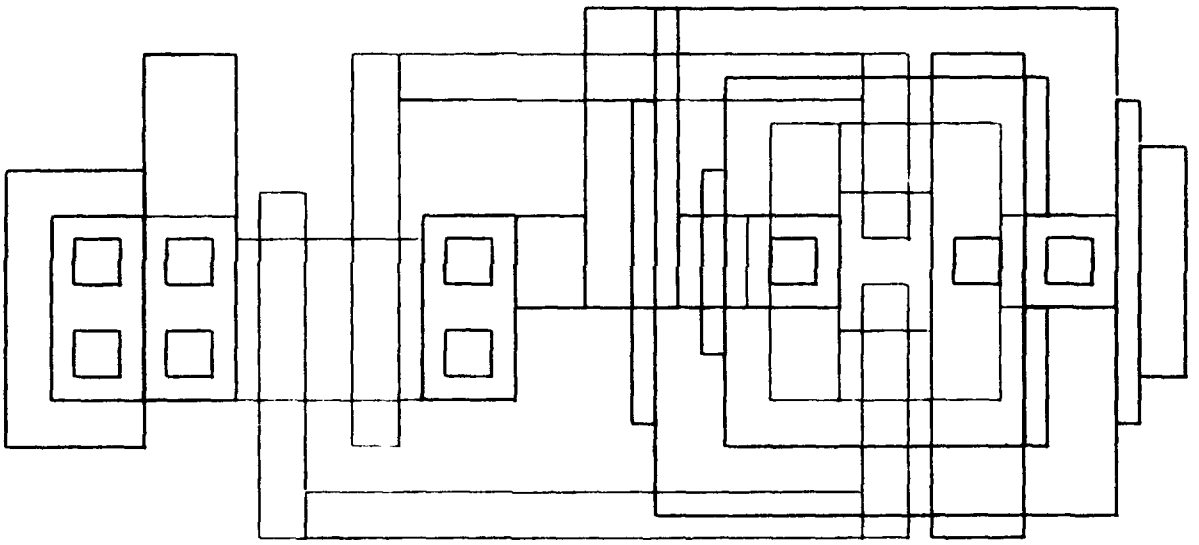


Figure ApC 5 The 2 Input NOR Gate Used in The Clock Circuit

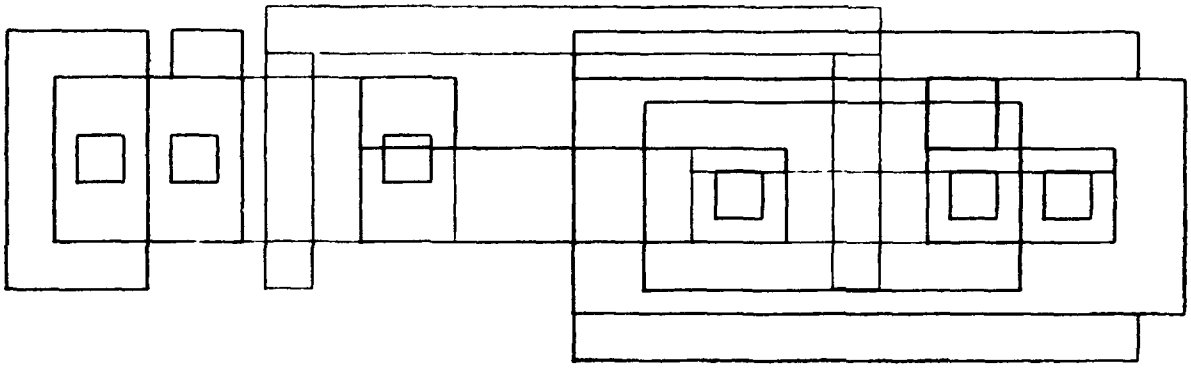


Figure ApC 6 The Inverter Cell Layout Geometry

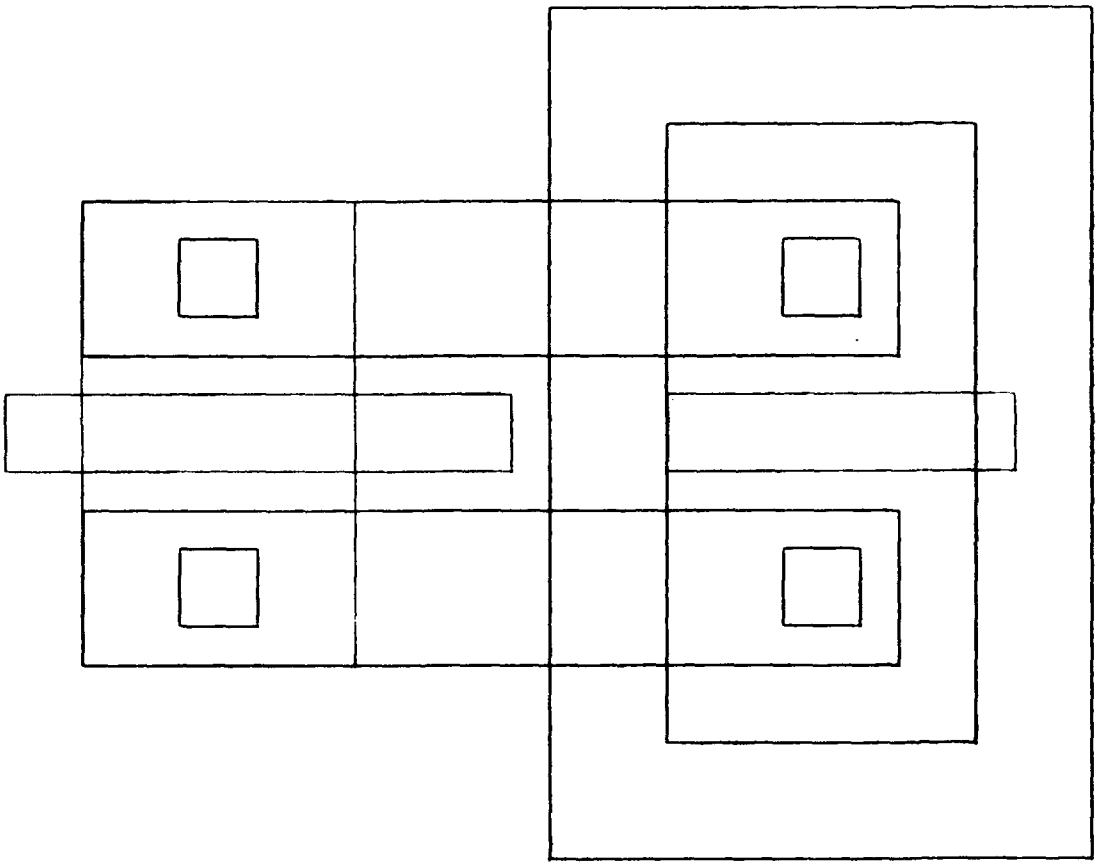


Figure ApC 7 Layout Geometry Of The Elementary Transmission Gate Used As Selective Switch For The Programmability Features Of The Chip

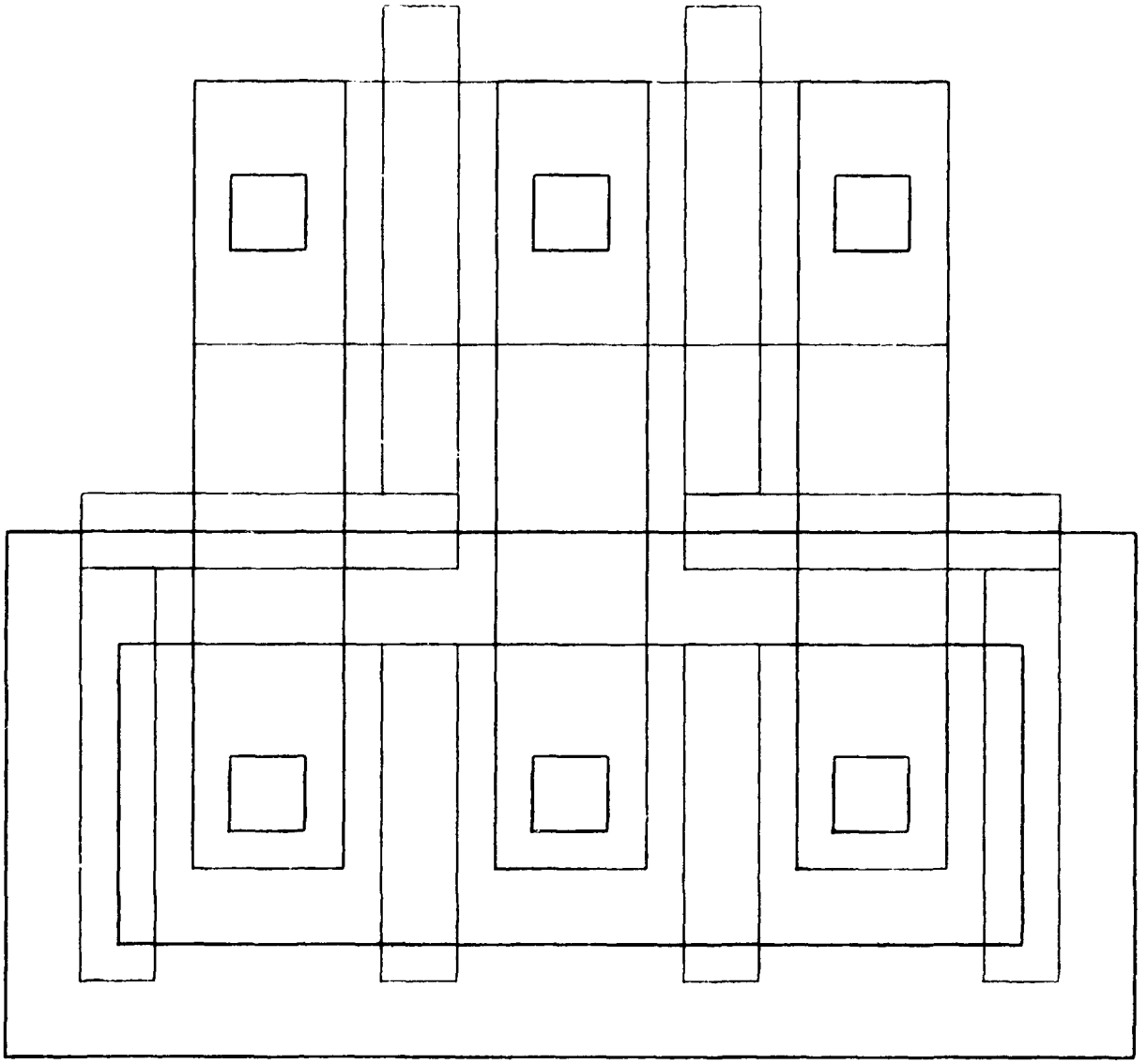


Figure ApC 8 Layout Geometry Of The Transmission Gate Used As The Switch In The Implementation Of The TSI And MOFR Damping

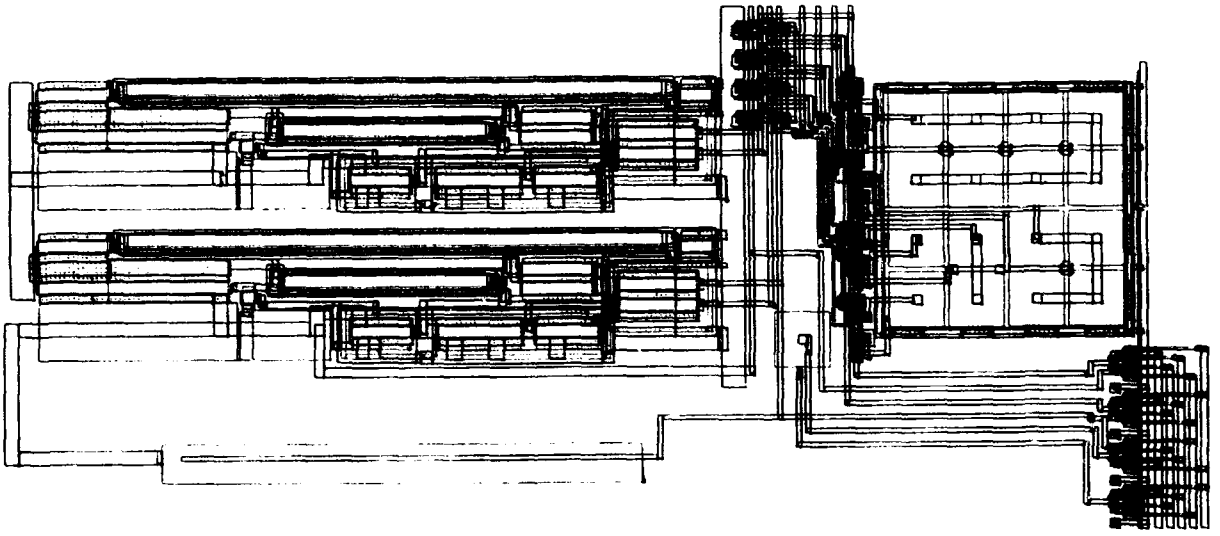


Figure ApC 9 The Composite Amplifier C2OA - 1 MOFR Cell Layout Geometry

APPENDIX D

A. SPICE 3C Simulation for the C - 2OA - 1 TSI composite amplifier
Results to the plots of the Figures 7.7 and 7.8

```
** SPICE file created for circuit compamp1
** Technology: scmos
** Orbit.nwell analog simulation parameters
* March 1994
* filename : comp1.cir
* submitted by Raphael Anestis

* ****************************************************************
* N37C SPICE LEVEL 2 PARAMETERS

.MODEL CMOSN NMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=1
+ VTO=0.8673 DELTA=4.9450E+00 LD=3.5223E-07 KP=4.6728E-05
+ UO=569.7 UEXP=1.7090E-01 UCRIT=5.9350E+04 RSH=1.9090E+01
+ GAMMA=0.4655 NSUB=4.3910E+15 NFS=1.980E+11 VMAX=5.7510E+04
+ LAMBDA=3.9720E-02 CGDO=4.3332E-10 CGSO=4.3332E-10
+ CGBO=3.5977E-10 CJ=1.0096E-04 MJ=0.8119 CJSW=4.6983E-10
+ MJSW=0.323107 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -9.0180E-08

.MODEL CMOSP PMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9506 DELTA=4.5950E+00 LD=3.7200E-07 KP=1.6454E-05
+ UO=200.6 UEXP=2.6690E-01 UCRIT=7.9260E+04 RSH=4.9920E+01
+ GAMMA=0.6561 NSUB=8.7250E+15 NFS=3.27E+11 VMAX=9.9990E+05
+ LAMBDA=4.5950E-02 CGDO=4.5769E-10 CGSO=4.5769E-10
+ CGBO=3.8123E-10 CJ=3.1469E-04 MJ=0.5687 CJSW=3.1456E-10
+ MJSW=0.275802 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.2400E-07

* ****************************************************************************

* First set of 2 pass gates (switches) - The ACR TSI (right side)
* The 111 is connected to the vin- of A2

* IN1 IN2 OUT P1 P2 NP1 NP2
* 0 111 108 115 114 113 110

M16 108 110 111 132 CMOSP L=2.0U W=7.0U
M17 0 113 108 132 CMOSP L=2.0U W=7.0U
```

```
M18 108 114 111 129 CMOSN L=2.0U W=4.0U
M19 0 115 108 129 CMOSN L=2.0U W=4.0U

* ************************************************************************

* Second set of 2 pass gates (switches) - The ACR TSI (left side)
* The 116 is connected in the middle of the 2 TSI's

* IN1 IN2 OUT P1 P2 NP1 NP2
* 116 0 109 115 114 113 110


M20 109 110 0 132 CMOSP L=2.0U W=7.0U
M21 116 113 109 132 CMOSP L=2.0U W=7.0U
M22 109 114 0 129 CMOSN L=2.0U W=4.0U
M23 116 115 109 129 CMOSN L=2.0U W=4.0U

* ************************************************************************
* The capacitor of the ACR TSI
* Simulation programmable ratio A set to 1

CA 109 108 6P

* ************************************************************************
* ************************************************************************
* Third set of 2 pass gates (switches) - The CR TSI (right side)
* Again the 116 is connected in the middle of the 2 TSI's


* IN1 IN2 OUT P1 P2 NP1 NP2
* 0 116 117 115 114 113 110

M24 117 110 116 132 CMOSP L=2.0U W=7.0U
M25 0 113 117 132 CMOSP L=2.0U W=7.0U
M26 117 114 116 129 CMOSN L=2.0U W=4.0U
M27 0 115 117 129 CMOSN L=2.0U W=4.0U

* ************************************************************************

* Fourth set of 2 pass gates (switches) - The CR TSI (left side)
* The 119 is connected to the vin+ of A2

* IN1 IN2 OUT P1 P2 NP1 NP2
* 119 0 118 115 114 113 110

M28 118 110 0 132 CMOSP L=2.0U W=7.0U
```

```
M29 119 113 118 132 CMOSP L=2.0U W=7.0U
M30 118 114 0 129 CMOSN L=2.0U W=4.0U
M31 119 115 118 129 CMOSN L=2.0U W=4.0U

* ********************************************************************
* The capacitor of the CR TSI

C 118 117 6P

* ********************************************************************
* ********************************************************************
* SUBCIRCUIT DEFINITION FOR THE TWO PHASE NON OVERLAPPING CLOCK


.SUBCKT CLOCK 310 300 309 301 311

* 310 = master clock , 300 = P1 , 309 = P2 ,
* 301 = NP1 , 311 = NP2

* N37C SPICE LEVEL 2 PARAMETERS

.MODEL CMOSN NMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=1
+ VTO=0.8673 DELTA=4.9450E+00 LD=3.5223E-07 KP=4.6728E-05
+ UO=569.7 UEXP=1.7090E-01 UCRIT=5.9350E+04 RSH=1.9090E+01
+ GAMMA=0.4655 NSUB=4.3910E+15 NFS=1.980E+11 VMAX=5.7510E+04
+ LAMBDA=3.9720E-02 CGDO=4.3332E-10 CGSO=4.3332E-10
+ CGBO=3.5977E-10 CJ=1.0096E-04 MJ=0.8119 CJSW=4.6983E-10
+ MJSW=0.323107 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -9.0180E-08

.MODEL CMOSP PMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9506 DELTA=4.5950E+00 LD=3.7200E-07 KP=1.6454E-05
+ UO=200.6 UEXP=2.6690E-01 UCRIT=7.9260E+04 RSH=4.9920E+01
+ GAMMA=0.6561 NSUB=8.7250E+15 NFS=3.27E+11 VMAX=9.9990E+05
+ LAMBDA=4.5950E-02 CGDO=4.5769E-10 CGSO=4.5769E-10
+ CGBO=3.8123E-10 CJ=3.1469E-04 MJ=0.5687 CJSW=3.1456E-10
+ MJSW=0.275802 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.2400E-07

* %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

* Power supplies
VDD 132 0 5
VSS 129 0 -5
```

```
M0 300 301 132 132 CMOSP L=2.0U W=28.0U
M1 129 301 300 129 CMOSN L=2.0U W=12.0U
M2 301 304 132 132 CMOSP L=2.0U W=28.0U
M3 129 304 301 129 CMOSN L=2.0U W=12.0U
M4 304 305 132 132 CMOSP L=2.0U W=14.0U
M5 129 305 304 129 CMOSN L=2.0U W=6.0U
M6 305 306 132 132 CMOSP L=2.0U W=14.0U
M7 129 306 305 129 CMOSN L=2.0U W=6.0U
M8 132 307 308 132 CMOSP L=2.0U W=7.0U
M9 308 309 306 132 CMOSP L=2.0U W=7.0U
M10 306 307 129 129 CMOSN L=2.0U W=3.0U
M11 306 309 129 129 CMOSN L=2.0U W=3.0U
M12 307 310 132 132 CMOSP L=2.0U W=7.0U
M13 129 310 307 129 CMOSN L=2.0U W=3.0U
M14 309 311 132 132 CMOSP L=2.0U W=28.0U
M15 129 311 309 129 CMOSN L=2.0U W=12.0U
M16 311 312 132 132 CMOSP L=2.0U W=28.0U
M17 129 312 311 129 CMOSN L=2.0U W=12.0U
M18 312 313 132 132 CMOSP L=2.0U W=14.0U
M19 129 313 312 129 CMOSN L=2.0U W=6.0U
M20 313 314 132 132 CMOSP L=2.0U W=14.0U
M21 129 314 313 129 CMOSN L=2.0U W=6.0U
M22 132 310 315 132 CMOSP L=2.0U W=7.0U
M23 315 300 314 132 CMOSP L=2.0U W=7.0U
M24 314 310 129 129 CMOSN L=2.0U W=3.0U
M25 314 300 129 129 CMOSN L=2.0U W=3.0U

* ********************************************************************

* PARASITIC CAPACITANCES FOR THE CLOCK CIRCUIT

** NODE: 315 = 2_input_nor_1/8_33_14#
C0 314 129 60F
** NODE: 314 = inverter2_0/IN
C1 313 129 68F
** NODE: 313 = inverter2_1/IN
C2 312 129 68F
** NODE: 312 = inverter4_2/IN
C3 129 129 266F
** NODE: 129 = Vss
C4 309 129 125F
** NODE: 309 = P2
C5 311 129 118F
** NODE: 311 = NP2
C6 310 129 28F
```

```
** NODE: 310 = CLK
** NODE: 308 = 2_input_nor_0/8_33_14#
C7 307 129 50F
** NODE: 307 = inverter_8/OUT
C8 306 129 60F
** NODE: 306 = inverter2_2/IN
C9 305 129 68F
** NODE: 305 = inverter2_3/IN
C10 304 129 68F
** NODE: 304 = inverter4_0/IN
C11 300 129 121F
** NODE: 300 = P1
C12 132 129 330F
** NODE: 132 = Vdd
C13 301 129 121F
** NODE: 301 = NP1
** NODE: 0 = GND!
** NODE: 1 = Vdd!

.ENDS CLOCK


* ********************************************************************************
* CMOS AMPLIFIER A2

* M57 130 131 130 2 ecap L=29.0U W=392.0U

* COMPENSATION CAPACITOR CC2 of A2
CC2 130 131 5P

* output = 131 = output of the composite
* inverting input = 111 =output of A1 and its feedback capacitor
* non-inverting input = 119 = point a of the composite (+)


M58 132 133 131 132 CMOSP L=10.0U W=164.0U
M59 134 134 132 132 CMOSP L=10.0U W=60.0U
M60 133 129 130 132 CMOSP L=10.0U W=10.0U
M61 131 135 129 129 CMOSN L=9.0U W=50.0U
M62 135 136 129 129 CMOSN L=10.0U W=71.0U
M63 132 133 135 129 CMOSN L=176.0U W=10.0U
M64 137 136 129 129 CMOSN L=10.0U W=53.0U
M65 132 138 133 132 CMOSP L=10.0U W=60.0U
M66 138 138 132 132 CMOSP L=10.0U W=60.0U
M67 137 119 133 129 CMOSN L=10.0U W=66.0U
M68 138 111 137 129 CMOSN L=10.0U W=66.0U
```

```
M69 134 134 136 129 CMOSN L=460.0U W=10.0U
M70 129 136 136 129 CMOSN L=10.0U W=27.0U

* ************************************************************************

* CMOS AMPLIFIER A1

* M71 139 111 139 2 ecap L=29.0U W=392.0U

* COMPENSATION CAPACITOR CC1 of A1
CC1 139 111 5P

* Output = 111 = inverting input of A2 = output of feedback capac.
* inverting input = 116 = input of feedback cap.= middle of switches
* non-inverting input = 146 = point b of the composite (-)

M72 132 140 111 132 CMOSP L=10.0U W=164.0U
M73 141 141 132 132 CMOSP L=10.0U W=60.0U
M74 140 129 139 132 CMOSP L=10.0U W=10.0U
M75 111 142 129 129 CMOSN L=9.0U W=50.0U
M76 142 143 129 129 CMOSN L=10.0U W=71.0U
M77 132 140 142 129 CMOSN L=176.0U W=10.0U
M78 144 143 129 129 CMOSN L=10.0U W=53.0U
M79 132 145 140 132 CMOSP L=10.0U W=60.0U
M80 145 145 132 132 CMOSP L=10.0U W=60.0U
M81 144 146 140 129 CMOSN L=10.0U W=66.0U
M82 145 116 144 129 CMOSN L=10.0U W=66.0U
M83 141 141 143 129 CMOSN L=460.0U W=10.0U
M84 129 143 143 129 CMOSN L=10.0U W=27.0U

* ************************************************************************

* PARASITIC CAPACITANCES FOR THE TWO CMOS AMPLIFIERS
* AND THEIR CONNECTIONS INSIDE THE CHIP

* M85 111 116 111 0 ecap L=44.0U W=466.0U
CF1 116 111 6P

* Different from the individual CMOS amplifier A1

C0 116 129 955F
** NODE: 116 = INCFvin-of A1
C1 146 129 22F
** NODE: 146 = cmosopamp2_0/Vin+ of A1

* ********************************************
```

```
* Same like the individual CMOS amplifier A1

C2 145 129 259F
** NODE: 145 = cmosopamp2_0/8_10_24#
C3 144 129 235F
** NODE: 144 = cmosopamp2_0/8_45_30#
C4 143 129 118F
** NODE: 143 = cmosopamp2_0/8_65_26#
C5 142 129 192F
** NODE: 142 = cmosopamp2_0/8_63_340#

* ************************************************
* Applies to connection between A1 and A2

C6 111 129 1374F
** NODE: 111 = OUTCF = OUTA1 = vin of A2

* ************************************************
* Same like the individual CMOS amplifier A1

C7 139 129 119F
** NODE: 139 = cmosopamp2_0/8_103_488#
C8 141 129 436F
** NODE: 141 = cmosopamp2_0/8_80_83#
C9 140 129 381F
** NODE: 140 = cmosopamp2_0/8_33_141#

* ************************************************
* Applies to connections of A2

C10 129 129 921F
** NODE: 129 = inverter_3/Vss
C11 119 129 89F
** NODE: 119 = transgate_3/IN1 = vin+ of A2


* ************************************************
* Same like the individual CMOS amplifier A2


C12 138 129 259F
** NODE: 138 = cmosopamp2_1/8_10_24#
C13 137 129 235F
** NODE: 137 = cmosopamp2_1/8_45_30#
C14 136 129 118F
** NODE: 136 = cmosopamp2_1/8_65_26#
```

```
C15 135 129 192F
** NODE: 135 = cmosopamp2_1/8_63_340#

* ***************************************************************
* Applies to connections of A2


C16 132 129 1385F
** NODE: 132 = cmosopamp2_1/Vdd
C17 131 129 974F
** NODE: 131 = OUTA2


* ***************************************************************
* Same like the individual CMOS amplifier A2

C18 130 129 119F
** NODE: 130 = cmosopamp2_1/8_103_488#
C19 134 129 436F
** NODE: 134 = cmosopamp2_1/8_80_83#
C20 133 129 381F
** NODE: 133 = cmosopamp2_1/8_33_141#

* ***************************************************************
* Applies to the CR capacitor between switches


C21 117 129 141F
** NODE: 117 = INCR
C22 118 129 97F
** NODE: 118 = OUTCR

* ***************************************************************
* C23 126 129 102F
** NODE: 126 = tgate1_7/NP2
* C24 127 129 78F
** NODE: 127 = tgate1_7/P2
* C25 124 129 90F
** NODE: 124 = tgate1_5/NP2
* C26 125 129 63F
** NODE: 125 = tgate1_5/P2
* C27 122 129 51F
** NODE: 122 = tgate1_3/NP2
* C28 123 129 45F
** NODE: 123 = tgate1_3/P2
```

```
* C29 120 129 68F
** NODE: 120 = tgate1_1/NP2
* C30 128 129 68F
** NODE: 128 = inverter_3/Vdd
* C31 121 129 37F
** NODE: 121 = tgate1_1/P2
* C32 107 129 113F
** NODE: 107 = tgate1_7/IN2
* C33 105 129 205F
** NODE: 105 = tgate1_5/IN2
* C34 100 129 173F
** NODE: 100 = tgate1_2/IN2
* C35 101 129 373F
** NODE: 101 = tgate1_3/IN2
* ********************************************************************

* Applies to the capacitor ACR between the switches


C36 108 129 214F
** NODE: 108 = INACR
C38 109 129 272F
** NODE: 109 = OUTACR

* ********************************************************************

* C37 102 129 300F
** NODE: 102 = tgate1_1/IN2
* C39 103 129 712F
** NODE: 103 = tgate1_0/IN2

C40 115 129 76F
** NODE: 115 = transgate_3/P1
C41 114 129 85F
** NODE: 114 = transgate_3/P2

* C42 112 129 167F
** NODE: 112 = transgate_3/IN2

C43 113 129 117F
** NODE: 113 = transgate_3/NP1
C44 110 129 129F
** NODE: 110 = transgate_3/NP2
** NODE: 1 = Vdd!

* C45 147 129 94F
```

```
** NODE: 147 = 6_35_321# ===FLOATING===
* C46 106 129 65F
** NODE: 106 = tgate1_6/IN2
* C47 104 129 99F
** NODE: 104 = tgate1_4/IN2
** NODE: 0 = GND!
* ********************************************************************

* ********************************************************************

* Power supplies for the chip

VDD 132 0 5
VSS 129 0 -5

* Main circuit

X1 310 115 114 113 110 CLOCK

* Signal supplies for the master clock circuit
VCLK 310 0 PULSE (5 -5 0.0us 2ns 2ns 0.5us 1.0us)

VINV 400 0 SIN(0 0.1 350KHz)
* VINV 400 0 AC 0.0001
* VINV 400 0 PULSE(1 -1 4us 2ns 2ns 10us 20us)
VNONINV 119 0 0

* Feedback in the negative configuration ( Attention ! of the composite )
* It is the vin+ of A1

RF 131 146 100K
RIN 400 146 10K


* ********************************************************************

.TRAN .0002us 20us
* .AC LIN 20 1 100000K
* .PROBE
.END
```

B. SPICE3C Simulation of the CMOS operational amplifier which was used in both configurations (TSI and MOFR), for the VLSI implementation of the composite amplifier C2OA - 1

Results to the plots of the Figure 7.9

```
** SPICE file created for circuit cmosopamp2
** Technology: scmos
** orbit.nwell analog fabrication parameters
*  March 1994
*  filename : cmosopamp2
*  submitted by Raphael Anestis

* ***************************************************************
* N37C  SPICE LEVEL 2 PARAMETERS

.MODEL CMOSN NMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=1
+ VTO=0.8673 DELTA=4.9450E+00 LD=3.5223E-07 KP=4.6728E-05
+ UO=569.7 UEXP=1.7090E-01 UCRIT=5.9350E+04 RSH=1.9090E+01
+ GAMMA=0.4655 NSUB=4.3910E+15 NFS=1.980E+11 VMAX=5.7510E+04
+ LAMBDA=3.9720E-02 CGDO=4.3332E-10 CGSO=4.3332E-10
+ CGBO=3.5977E-10 CJ=1.0096E-04 MJ=0.8119 CJSW=4.6983E-10
+ MJSW=0.323107 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -9.0180E-08

.MODEL CMOSP PMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9506 DELTA=4.5950E+00 LD=3.7200E-07 KP=1.6454E-05
+ UO=200.6 UEXP=2.6690E-01 UCRIT=7.9260E+04 RSH=4.9920E+01
+ GAMMA=0.6561 NSUB=8.7250E+15 NFS=3.27E+11 VMAX=9.9990E+05
+ LAMBDA=4.5950E-02 CGDO=4.5769E-10 CGSO=4.5769E-10
+ CGBO=3.8123E-10 CJ=3.1469E-04 MJ=0.5687 CJSW=3.1456E-10
+ MJSW=0.275802 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.2400E-07

* ***************************************************************

* Power supplies
VDD 102 0 5
VSS 105 0 -5
VINVERT 111 0 AC 0.0001
VNONINVERT 110 0 0
* VIN 111 0 PULSE(1 -1 4us 2ns 2ns 10us 20us)
* VINV 400 0 SIN(0 0.1 10KHz)
```

```
RF 101 111 100K
RIN 111 400 10K


** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
** M0 100 101 100 0 ecap L=29.0U W=392.0U

M1 102 103 101 102 CMOSP L=10.0U W=164.0U
M2 104 104 102 102 CMOSP L=10.0U W=60.0U
M3 103 105 100 102 CMOSP L=10.0U W=10.0U
M4 101 106 105 105 CMOSN L=9.0U W=50.0U
M5 106 107 105 105 CMOSN L=10.0U W=71.0U
M6 102 103 106 105 CMOSN L=176.0U W=10.0U
M7 108 107 105 105 CMOSN L=10.0U W=53.0U
M8 102 109 103 102 CMOSP L=10.0U W=60.0U
M9 109 109 102 102 CMOSP L=10.0U W=60.0U
M10 108 110 103 105 CMOSN L=10.0U W=66.0U
M11 109 111 108 105 CMOSN L=10.0U W=66.0U
M12 104 104 107 105 CMOSN L=460.0U W=10.0U
M13 105 107 107 105 CMOSN L=10.0U W=27.0U

* Compensation capacitor CC
CC 100 101 5P


C0 101 105 12F
C1 105 105 375F

** NODE: 105 = Vss
** NODE: 111 = Vin-
** NODE: 110 = Vin+
C2 109 105 259F
** NODE: 109 = 8_10_24#
C3 108 105 235F
** NODE: 108 = 8_45_30#
C4 107 105 118F
** NODE: 107 = 8_65_26#
C5 106 105 192F
** NODE: 106 = 8_63_340#
C6 102 105 657F
** NODE: 102 = Vdd
C7 101 105 954F
** NODE: 101 = 8_99_492#
C8 100 105 119F
```

```
** NODE: 100 = 8_103_488#
C9 104 105 436F
** NODE: 104 = 8_80_83#
C10 103 105 381F
** NODE: 103 = 8_33_141#
** NODE: 0 = GND!
** NODE: 1 = Vdd!

* ********************************************************************************

*.AC DEC 20 1 100000K
.TRAN .0002us 100us
.PROBE
.END
```

C. SPICE3C Simulation for the two phase non - overlapping clock that whose purpose was to provide the appropriate switching in both configurations (TSI and MOFR) for the VLSI implementation of the composite amplifier C2OA - 1
Results to the plots of the Figure 7.6

```
** SPICE file created for circuit nvclk2
** Technology: scmos
** orbit.nwell analog fabrication parameters
*  March 1994
*  filename : ph2nvclk = 2 phase non overlapping clock
*  submitted by Raphael Anestis

*********************************************************************
* N37C  SPICE LEVEL 2 PARAMETERS

.MODEL CMOSN NMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=1
+ VTO=0.8673 DELTA=4.9450E+00 LD=3.5223E-07 KP=4.6728E-05
+ UO=569.7 UEXP=1.7090E-01 UCRIT=5.9350E+04 RSH=1.9090E+01
+ GAMMA=0.4655 NSUB=4.3910E+15 NFS=1.980E+11 VMAX=5.7510E+04
+ LAMBDA=3.9720E-02 CGDO=4.3332E-10 CGSO=4.3332E-10
+ CGBO=3.5977E-10 CJ=1.0096E-04 MJ=0.8119 CJSW=4.6983E-10
+ MJSW=0.323107 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -9.0180E-08

.MODEL CMOSP PMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9506 DELTA=4.5950E+00 LD=3.7200E-07 KP=1.6454E-05
+ UO=200.6 UEXP=2.6690E-01 UCRIT=7.9260E+04 RSH=4.9920E+01
+ GAMMA=0.6561 NSUB=8.7250E+15 NFS=3.27E+11 VMAX=9.9990E+05
+ LAMBDA=4.5950E-02 CGDO=4.5769E-10 CGSO=4.5769E-10
+ CGBO=3.8123E-10 CJ=3.1469E-04 MJ=0.5687 CJSW=3.1456E-10
+ MJSW=0.275802 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.2400E-07

* *********************************************************************

* Power supplies

VDD 102 0 5
VSS 103 0 -5
* VCLK 110 0 SIN(0 5 100KHz)
VIN 110 0 PULSE (5 -5 0.1us 2ns 2ns 0.5us 1.0us)

* *********************************************************************
```

```
* Circuit extracted with ext2spice from the equivalent Magic file

** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M0 100 101 102 102 CMOSP L=2.0U W=28.0U
M1 103 101 100 103 CMOSN L=2.0U W=12.0U
M2 101 104 102 102 CMOSP L=2.0U W=28.0U
M3 103 104 101 103 CMOSN L=2.0U W=12.0U
M4 104 105 102 102 CMOSP L=2.0U W=14.0U
M5 103 105 104 103 CMOSN L=2.0U W=6.0U
M6 105 106 102 102 CMOSP L=2.0U W=14.0U
M7 103 106 105 103 CMOSN L=2.0U W=6.0U
M8 102 107 108 102 CMOSP L=2.0U W=7.0U
M9 108 109 106 102 CMOSP L=2.0U W=7.0U
M10 106 107 103 103 CMOSN L=2.0U W=3.0U
M11 106 109 103 103 CMOSN L=2.0U W=3.0U
M12 107 110 102 102 CMOSP L=2.0U W=7.0U
M13 103 110 107 103 CMOSN L=2.0U W=3.0U
M14 109 111 102 102 CMOSP L=2.0U W=28.0U
M15 103 111 109 103 CMOSN L=2.0U W=12.0U
M16 111 112 102 102 CMOSP L=2.0U W=28.0U
M17 103 112 111 103 CMOSN L=2.0U W=12.0U
M18 112 113 102 102 CMOSP L=2.0U W=14.0U
M19 103 113 112 103 CMOSN L=2.0U W=6.0U
M20 113 114 102 102 CMOSP L=2.0U W=14.0U
M21 103 114 113 103 CMOSN L=2.0U W=6.0U
M22 102 110 115 102 CMOSP L=2.0U W=7.0U
M23 115 100 114 102 CMOSP L=2.0U W=7.0U
M24 114 110 103 103 CMOSN L=2.0U W=3.0U
M25 114 100 103 103 CMOSN L=2.0U W=3.0U
** NODE: 115 = 2_input_nor_1/8_33_14#
C0 114 103 60F
** NODE: 114 = inverter2_0/IN
C1 113 103 68F
** NODE: 113 = inverter2_1/IN
C2 112 103 68F
** NODE: 112 = inverter4_2/IN
C3 103 103 266F
** NODE: 103 = Vss
C4 109 103 125F
** NODE: 109 = P2
C5 111 103 118F
** NODE: 111 = NP2
C6 110 103 28F
** NODE: 110 = CLK
```

```
** NODE: 108 = 2_input_nor_0/8_33_14#
C7 107 103 50F
** NODE: 107 = inverter_8/OUT
C8 106 103 60F
** NODE: 106 = inverter2_2/IN
C9 105 103 68F
** NODE: 105 = inverter2_3/IN
C10 104 103 68F
** NODE: 104 = inverter4_0/IN
C11 100 103 121F
** NODE: 100 = P1
C12 102 103 330F
** NODE: 102 = Vdd
C13 101 103 121F
** NODE: 101 = NP1
** NODE: 0 = GND!
** NODE: 1 = Vdd!

* ********************************************************************
.TRAN 10ns 2us
.PROBE
.END
```

D. SPICE3C Simulation for the inverters that were used as a main building block of the digital part of the fabricated microchip
Results to the plot of the Figure 7.5

```
** SPICE file created for circuit inverter4
** Technology: scmos
** orbit.nwell analog simulation parameters
*  March 1994
*  filename : inverter4.cir
*  submitted by Raphael Anestis

* ************************************************************************
* N37C  SPICE LEVEL 2 PARAMETERS

.MODEL CMOSN NMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=1
+ VTO=0.8673 DELTA=4.9450E+00 LD=3.5223E-07 KP=4.6728E-05
+ UO=569.7 UEXP=1.7090E-01 UCRIT=5.9350E+04 RSH=1.9090E+01
+ GAMMA=0.4655 NSUB=4.3910E+15 NFS=1.980E+11 VMAX=5.7510E+04
+ LAMBDA=3.9720E-02 CGDO=4.3332E-10 CGSO=4.3332E-10
+ CGBO=3.5977E-10 CJ=1.0096E-04 MJ=0.8119 CJSW=4.6983E-10
+ MJSW=0.323107 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -9.0180E-08

.MODEL CMOSP PMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9506 DELTA=4.5950E+00 LD=3.7200E-07 KP=1.6454E-05
+ UO=200.6 UEXP=2.6690E-01 UCRIT=7.9260E+04 RSH=4.9920E+01
+ GAMMA=0.6561 NSUB=8.7250E+15 NFS=3.27E+11 VMAX=9.9990E+05
+ LAMBDA=4.5950E-02 CGDO=4.5769E-10 CGSO=4.5769E-10
+ CGBO=3.8123E-10 CJ=3.1469E-04 MJ=0.5687 CJSW=3.1456E-10
+ MJSW=0.275802 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.2400E-07

* ************************************************************************
** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error

* Power supplies
VDS 102 103 5.0

* input signals
VIN 101 0
```

```
* Main circuit

M0 100 101 102 1 CMOSP L=2.0U W=28.0U
M1 103 101 100 0 CMOSN L=2.0U W=12.0U

C0 103 0 24F
** NODE: 103 = Vss
C1 100 0 96F
** NODE: 100 = OUT
C2 102 0 42F
** NODE: 102 = Vdd
** NODE: 101 = IN
** NODE: 0 = GND!
** NODE: 1 = Vdd!
* ********************************************************************************

* Simulation parameters
.DC VIN 0 5 0.01
.PROBE
.END
```

E. SPICE3C Simulation for the elementary transmission gate that was used in all switches of both configurations (TSI and MOFR), for the VLSI implementation of the composite amplifier C2OA - 1

This simulation is the analog check that the gate passes correctly ones and zeros
It is also simulated by ESIM , the plot is not included.

```
** SPICE file created for circuit tgate1
** Technology: scmos
** orbit.nwell analog fabrication parameters
*  March 1994
*  filename : tgate1
*  submitted by Raphael Anestis

* ***************************************************************
* N37C  SPICE LEVEL 2 PARAMETERS

.MODEL CMOSN NMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=1
+ VTO=0.8673 DELTA=4.9450E+00 LD=3.5223E-07 KP=4.6728E-05
+ UO=569.7 UEXP=1.7090E-01 UCRIT=5.9350E+04 RSH=1.9090E+01
+ GAMMA=0.4655 NSUB=4.3910E+15 NFS=1.980E+11 VMAX=5.7510E+04
+ LAMBDA=3.9720E-02 CGDO=4.3332E-10 CGSO=4.3332E-10
+ CGBO=3.5977E-10 CJ=1.0096E-04 MJ=0.8119 CJSW=4.6983E-10
+ MJSW=0.323107 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -9.0180E-08

.MODEL CMOSP PMOS LEVEL=2 PHI=0.600000 TOX=4.2100E-08 XJ=0.200000U TPG=-1
+ VTO=-0.9506 DELTA=4.5950E+00 LD=3.7200E-07 KP=1.6454E-05
+ UO=200.6 UEXP=2.6690E-01 UCRIT=7.9260E+04 RSH=4.9920E+01
+ GAMMA=0.6561 NSUB=8.7250E+15 NFS=3.27E+11 VMAX=9.9990E+05
+ LAMBDA=4.5950E-02 CGDO=4.5769E-10 CGSO=4.5769E-10
+ CGBO=3.8123E-10 CJ=3.1469E-04 MJ=0.5687 CJSW=3.1456E-10
+ MJSW=0.275802 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is -2.2400E-07

* ***************************************************************
* Power supplies
VP2 103 0 5.0
VNP2 101 0 0.0

* Input signals
VIN 102 0 PULSE (5 -5 0.1us 2ns 2ns 0.5us 1.0us)

* Main circuit
```

```
** NODE: 0 = GND
** NODE: 1 = Vdd
** NODE: 2 = Error
M0 100 101 102 1 CMOSP L=2.0U W=7.0U
M1 100 103 102 0 CMOSN L=2.0U W=4.0U
** NODE: 103 = P2
C0 100 0 29F
** NODE: 100 = OUT
C1 102 0 29F
** NODE: 102 = IN2
** NODE: 101 = NP2
** NODE: 0 = GND!
** NODE: 1 = Vdd!

* ********************************************************************
* Simulation parameters
.TRAN 10ns 2us
.PROBE
.END
```

LIST OF REFERENCES

1. Michael, S.N., *Composite Operational Amplifiers and Their Application in Active Networks,* Ph.D. Dissertation, West Virginia University, Morgantown, West Virginia, August 1993.

2. Mikhael, W.B. and Michael,S.N., "Composite Operational Amplifiers : Generation and Finite Gain Applications," *IEEE Transactions on Circuits and Systems,* v.CAS-34, No. 5. pp. 449-460, May 1987.

3. Mikhael, W.B. and Michael, S.N., "Inverting Integrator and Active Filter Applications of Composite Operational Amplifiers," in *IEEE Transactions on Circuits and Systems,* v.CAS-34, No. 5. pp. 461-470, May 1987.

4. Mikhael, W.B. and Michael, S.N., "A systematic General Approach for the Generation of Composite OAs With Some Useful Applications in Linear Active Networks," in *Proceedings of the 25th Midwest Symposium on Circuits and Systems,* pp. 454 - 463, Houston, Michigan, August 1982.

5. Mikhael, W.B. and Michael, S.N., "High Speed, High Accuracy Integrated Operational Amplifiers," in *Proceedings of the Midwest Symposium on Circuits and Systems,* Morgantown, West Virginia, June 1984.

6. Michael, S.N. and Mikhael, W.B., "Generation of Actively Compensated Composite Operational Amplifiers and Their Use in Extending the Operational Frequencies of Linear Active Networks," in *Proceedings of the IEEE Symposium on Circuits and Systems,* Newport Beach, California, May 1983.

7. Mikhael, W.B. and Michael, S.N., "Actively Compensated Composite Operational Amplifiers," in *Proceedings of the Midwest Symposium on Circuits and Systems,* Albuquerque, New Mexico, June 1981.

8. Bingham, E.W., *Stray Insensitive Switched Capacitor Composite Operational Amplifiers,* Master's Thesis, Naval Postgraduate School, Monterey, California, March 1993.

9. Gregorian, R. and Temes, G.C., *Analog MOS Integrated Circuits For Signal Processing,* John Wiley and Sons, Inc., New York, 1986.

10. Kollomorgan, G.S., *Generation of Programmable Composite Operational Amplifiers With a CMOS Integrated Circuit,* Master's Thesis, Naval Postgraduate School, Monterey, California, December 1986.

11. Weste, N.H. and Eshraghian, K., *Principles of CMOS VLSI Design,* Second Edition,Addison Wesley Publishing Co., Reading, Massachusetts,1993.

12. Glasser, L.A. and Dobberpuhl, D.W., *The Design and Analysis of VLSI circuits,*Addison Wesley Publishing Co., Reading, Massachusetts, 1988.

13. Ghausi, M.S. and Laker, K.R., *Modern Filter Design,* Prentice Hall, Englewood Cliffs, New Jersey, 1981.

14. Silvernagel, G.A., *VLSI implementation of Stray Insensitive Switched Capacitor Composite Operational Amplifiers,* Master's thesis, Naval Postgraduate School, Monterey, California, December 1993.

15. Gray, P.R. and Meyer, R.G., *Analysis and Design of Analog Integrated Circuits,* Third Edition, John Wiley & Sons Publishing Co., New York,1993.

16. Wolfram, S. *Mathematica System for Doing Mathematics by Computer,* Second Edition,Addison Wesley Publishing Co., Reading, Massachusetts, 1988.

17. Jurada, J.M., *Introduction to Artificial Neural Systems,* West Publishing Co., St. Paul, 1992.

18. Fenical, L.H., *PSpice a Tutorial,* Prentice Hall, Englewood Cliffs, New Jersey, 1992.

19. Sedra and Smith, *Microelectronic Circuits,* 3rd edition, Saunders College Publishing, Philadelphia, 1991

20. Strum, R.D. and Kirk, D.E., *First Principles of Discrete Systems and Digital Signal Processing,* Addison Wesley Publishing Co., Reading, Massachusetts, 1991.

21. Coughlin, R.F. and Driscoll, F.F., *Operational Amplifiers and Linear Integrated Circuits,* fourth edition, Prentice Hall, Englewood Cliffs, New Jersey, 1993.

22. Nagle, T. and Caroll, B.D., *An Introduction to Computer Logic,*Prentice Hall, Englewood Cliffs, New Jersey, 1988.

23. Wakerly, J.F., *Digital Design Principles and Practices,* Prentice Hall, Englewood Cliffs, New Jersey, 1991.

24. Taub, T., *Digital Circuits and Microprocessors,* McGraw Hill Publishing Co.,New York, 1988.

25. Cuo, B.C., *Automatic Control Systems,* Sixth Edition, Prentice Hall, Englewood Cliffs, New Jersey, 1987.

26. Siewiorek, D.P. and Swartz, R.S., *Reliable Computer Systems Design and Evaluation,* second edition, Digital Press, New York, 1992.

27. Leonard, N.H. and Levine, W.S., *Using MATLAB to Analyze and Design Control Systems,* Benjamin/Cummings Publishing Co., Redwood City, California, 1992.

28. Cannon, D.L., *Understanding Solid State Electronics,* 5th edition, SAMS series, Massachusetts, 1990.

29. Morgan, N., *Artificial Neural Networks-Electronic Implementations,* IEEE Computer Society Neural Networks Technology Series, Chicago, 1992.

30. Hovanessian, S.A., *Introduction to Sensor Systems,* Artech House, Norwood, Massachusetts, 1988.

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